Ordering number : ENA2177

LV5069JA

Bi-CMOS IC

Low power consumption and high efficiency Step-down Switching Regulator Controller

ON Semiconductor®

http://onsemi.com

Overview

LV5069JA is Step-down switching regulator controller. The recommended operating range is 4.5V-23V. The operating current is about 68µA, and low power consumption is achieved.

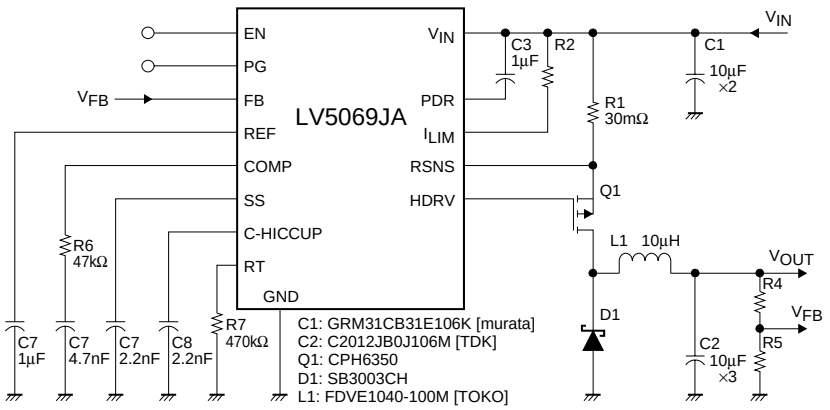
Features and Functions

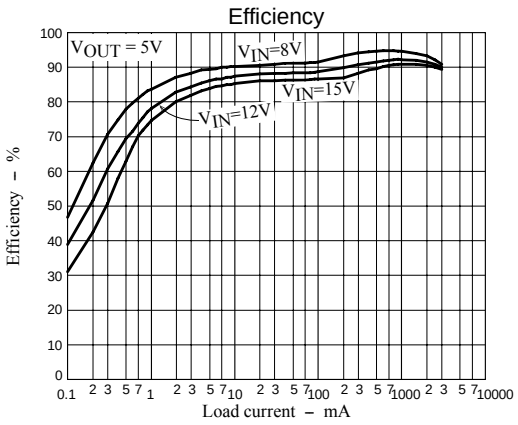
- Typical value of light load mode current is 68µA
- 4.5V to 23V Operating input voltage range
- The oscillatory frequency can be set by the external pin. The oscillatory frequency is 300kHz - 1MHz.
- Output voltage adjustable to 1.26V
- Built-in OCP circuit with P-by-P method
- When P-by-P is generated continuously, It shifts to the HICCUP operation
- If connect C-HICCUP to GND pin, Then latch-off when over current
- External capacitor Soft-Start
- Under voltage lock-out, Thermal shutdown and power good indication

Applications

- DVD/Blu-rayTM Drivers and HDD
- LCD Monitors and TVs
- Point of Load DC/DC Converters
- Office Supplies

Typical Application





Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Input voltage	V_{IN} max		25	V
Allowable pin voltage	PDR		V_{IN}	V
	V_{IN}-PDR		6	V
	HDRV		V_{IN}	V
	RSNS		V_{IN}	V
	I_{LIM}		V_{IN}	V
	EN		V_{IN}	V
	PG		V_{IN}	V
	REF		6	V
	RT		REF	V
	SS		REF	V
	FB		REF	V
	COMP		REF	V
	C-HICCUP		REF	V
Allowable power dissipation	Pd max	Specified substrate *1	0.74	W
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

*1 Specified substrate : 114.3mm × 76.1mm × 1.6mm, fiberglass epoxy printed circuit board

Caution 1) Absolute maximum ratings represent the values which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommendation Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Input voltage range	V_{IN}		4.5 to 23	V

Electrical Characteristics at Ta = 25°C, V_{IN} = 15V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Reference voltage]						
Internal reference voltage	V_{REF}		1.247	1.260	1.273	V
Pch drive voltage	V_{PDR}	I_{OUT} = 0 to -5mA	V_{IN}-5.5	V_{IN}-5.0	V_{IN}-4.5	V
[Saw wave oscillator]						
Oscillatory frequency	F_{OSC}	RT = 470kΩ	280	330	380	kHz
[ON/OFF circuit]						
IC startup voltage (EN PIN)	V_{CNT_ON}		2.0		V_{IN}	V
Disable voltage (EN PIN)	V_{CNT_OFF}				0.3	V
[Soft start circuit]						
Soft start source current	I_{SS_SC}	EN > 2V	1.3	2.0	2.7	µA
Soft start sink current	I_{SS_SK}	EN < 0.3V, SS = 0.4V	2	3	4	mA
[UVLO circuit]						
UVLO release voltage	V_{UVLON}	FB = COMP	3.3	3.7	4.1	V
UVLO lock voltage	V_{UVLOF}	FB = COMP	3.02	3.42	3.82	V
[Error amplifier]						
Input bias current	I_{EA_IN}		-100	-50	100	nA
Error amplifier gain	G_{EA}		100	250	400	µA/V
Output sink current	I_{EA_OSK}	FB = 1.75V	-40	-20	-10	µA
Output source current	I_{EA_OSC}	FB = 0.75V	10	20	40	µA

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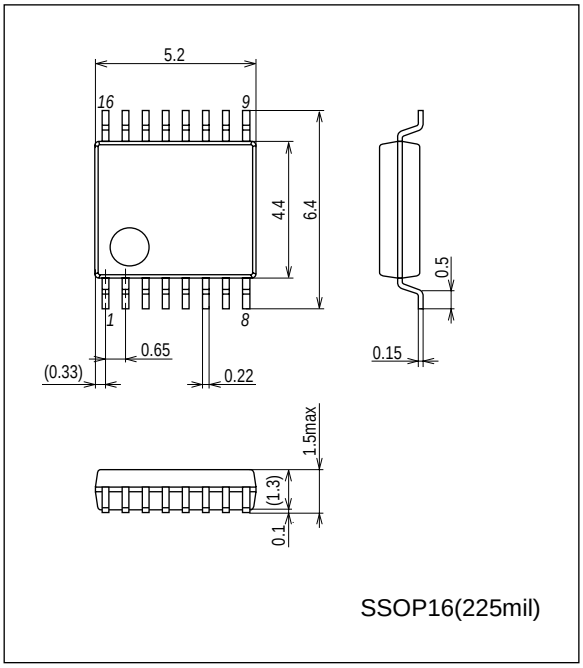
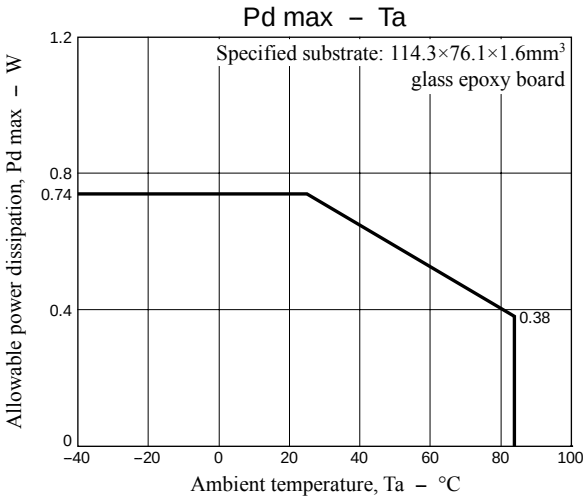
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Over current limit circuit]						
Reference current	I_{LIM}		48.4	55	61.6	μA
Over current detection comparator offset voltage	V_{LIM_OFS}		-5		5	mV
RSNS pin input range	V_{RSNS}		V_{IN}-0.23		V_{IN}	V
HICCUP timer start-up cycle	N_{CYC}			15		cycle
HICCUP comparator threshold voltage	V_{tHIC}		1.23	1.29	1.35	V
HICCUP timer charge current	I_{HIC}		1	2	3	μA
[PWM Comparator]						
Maximum on-duty	D_{MAX}	RT = 470kΩ	94			%
[Logic output]						
Power good “L” sink current	I_{PWRGD_L}	PG = 5V	4	5	6	mA
Power good “H” leakage current	I_{PWRGD_H}	PG = 5V			1	μA
Power good threshold voltage	V_{TPG}		1.0	1.1	1.2	V
Power good hysteresis	V_{PG_H}		40	50	60	mV
[Output]						
High side output on resistance	R_{ONH}			5		Ω
Low side output on resistance	R_{ONL}			9		Ω
High side output on current	I_{ONH}		300			mA
Low side output on current	I_{ONL}		150			mA
[The entire device]						
Standby current	I_{CCS}	EN < 0.3V			1	μA
Light load mode consumption current	I_{SLEEP}	EN > 2V No switching	48	68	88	μA
Thermal shutdown	TSD	*Design guarantee		170		°C

*Design guarantee: Signifies target value in design. These parameters are not tested in an independent IC.

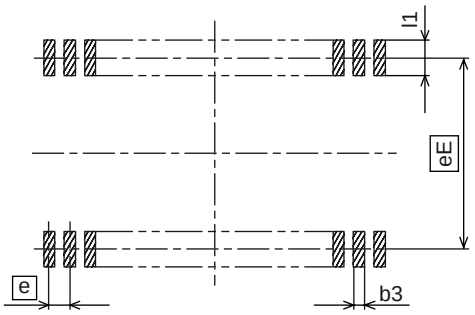
Package Dimensions

unit : mm (typ)
3178B





Mounting pad sketch

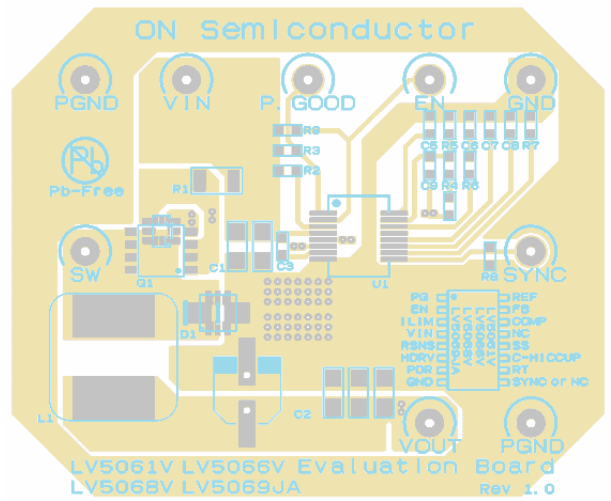


(Unit: mm)

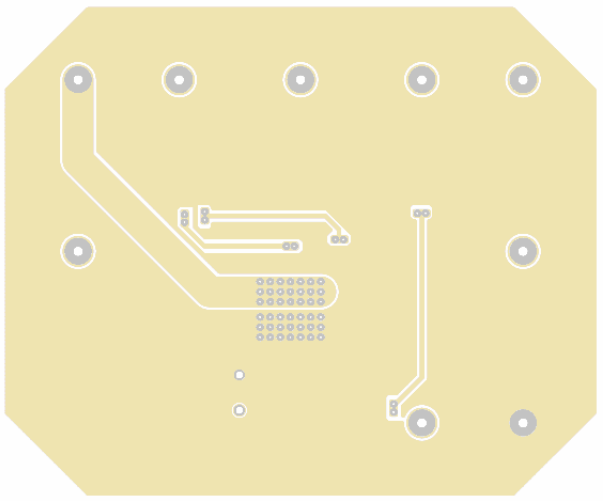
Reference symbol	SSOP16(225mil)
eE	5.80
e	0.65
b3	0.32
l1	1.00

Caution: The mounting pad sketch is a reference value, which is not a guaranteed value.

Evaluation Board Pattern diagram



Top

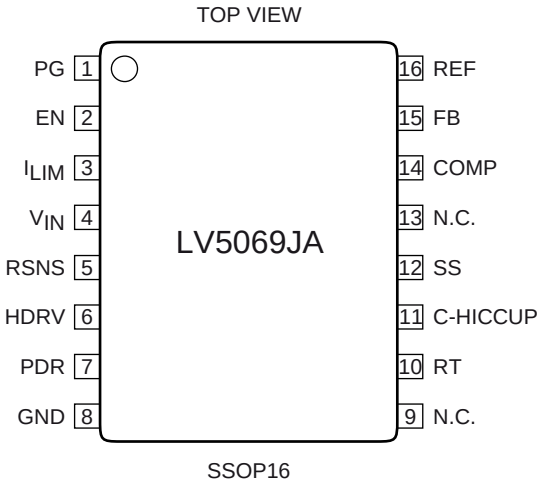


Bottom

2nd Layer

3rd Layer

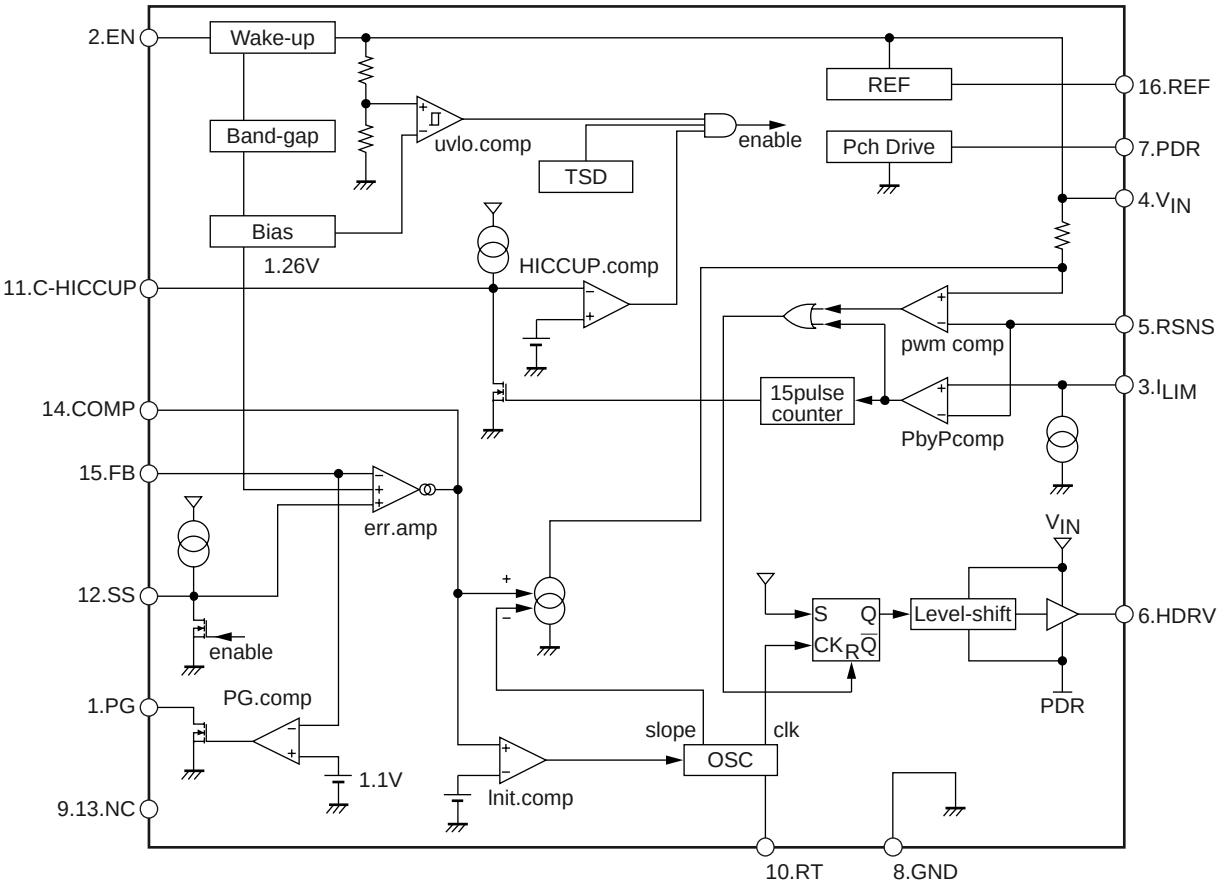
Pin Assignment



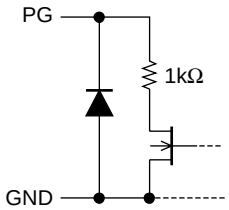
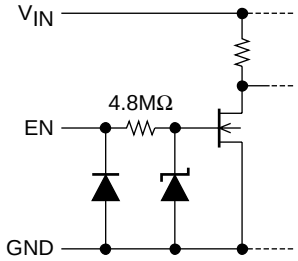
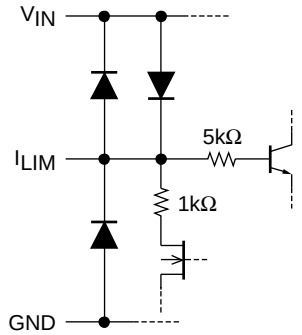
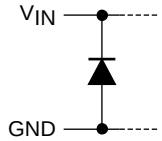
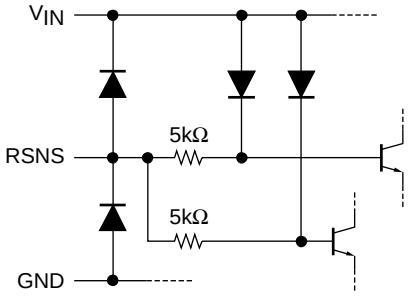
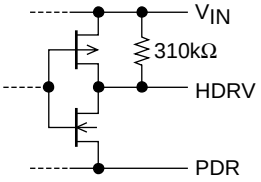
Pin Function Description

Pin No	Pin Name	Description
1	PG	Power good pin. Connect to open drain of MOS-FET in ICs inside. Setting output voltage to "L", when FB voltage is 1.05V or less.
2	EN	ON/OFF Pin.
3	I_{LIM}	For current detection. Sink current is about 55μA. The current limiter comparator works when an external resistor is connected between this pin and V_{IN}, and if the voltage of this resistor is less than the voltage of RSNS then Pch MOS is turned off. This operation is reset each PWM pulse.
4	V_{IN}	Supply voltage pin. It is observed by the UVLO function. When its voltage becomes 3.7V or more, ICs startup in soft start.
5	RSNS	Current detection resistor connection pin. Resistor is connected between V_{IN} and this pin, and the current flow to MOSFET is measured.
6	HDRV	The external high-side MOSFET gate drive pin.
7	PDR	Pch MOSFET gate drive voltage. The bypass capacitor is necessarily connected between this pin and V_{IN}.
8	GND	Ground Pin. Ground pin voltage is reference voltage
9	NC	NC Pin. The NC Pin becomes open in an IC.
10	RT	Oscillation frequency setting pin. Resistor is connected between this pin and GND.
11	C-HICCUP	It is capacitor connection pin for setting re-startup cycle in HICCUP mode. If connect it to GND pin, then latch-off when over current.
12	SS	Capacitor connection pin for soft start. About 2.0μA current charges the soft start capacitor.
13	NC	NC Pin. The NC Pin becomes open in an IC.
14	COMP	Error amplifier output pin. The phase compensation network is connected between GND pin and COMP pin. Thanks to current-mode control, comp pin voltage would tell you the output current amplitude. Comp pin is connected internally to an Init.comparator which compares with 0.9V reference. If comp pin voltage is larger than 0.9V, IC operates in “continuous mode”. If comp pin voltage is smaller than 0.9V, IC operates in “discontinuous mode (low consumption mode)”.
15	FB	Error amplifier reverse input pin. ICs make its voltage keep 1.26V. Output voltage is divided by external resistances and it across FB.
16	REF	Reference voltage.

Block Diagram



Pin Equivalent Circuit

Pin No.	Pin name	Equivalent circuit
1	PG	
2	EN	
3	I_{LIM}	
4	V_{IN}	
5	RSNS	
6	HDRV	

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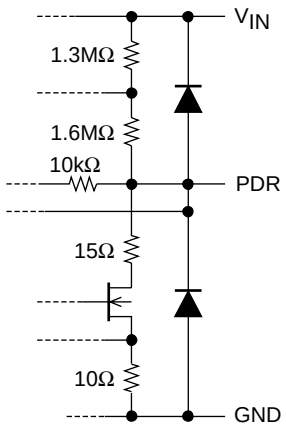
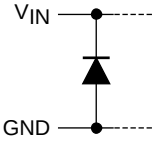
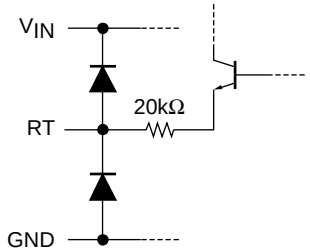
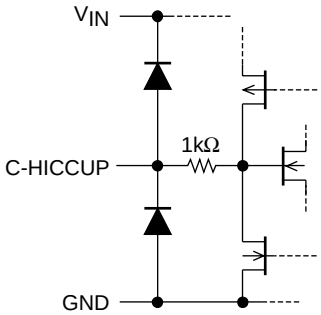
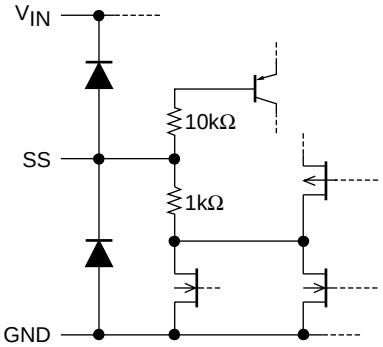
Pin No.	Pin name	Equivalent circuit
7	PDR	
8	GND	
9	NC	
10	RT	
11	C-HICCUP	
12	SS	
13	NC	

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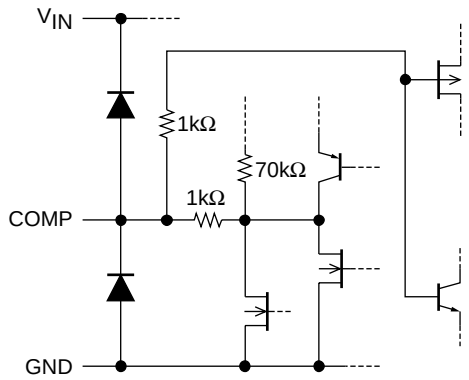
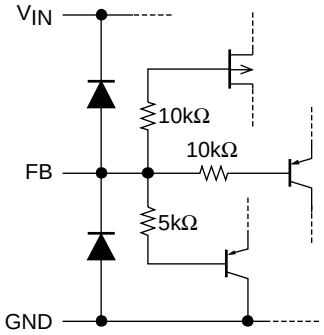
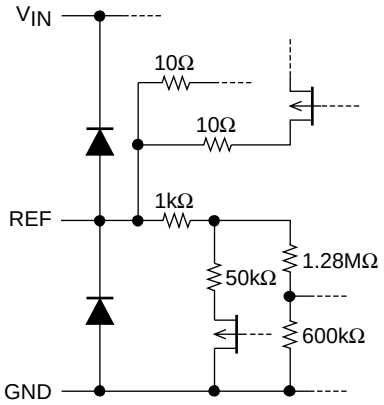
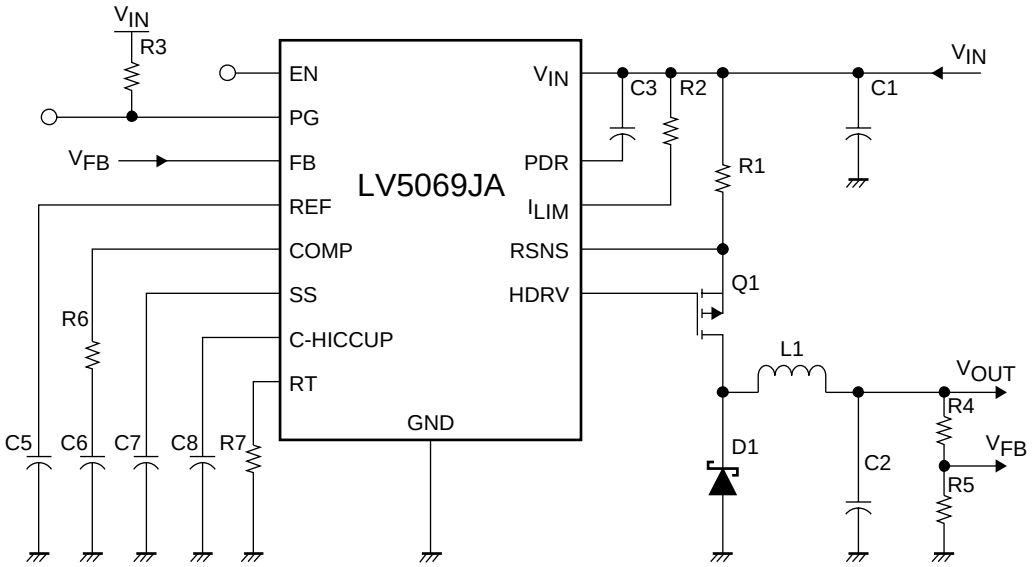
Pin No.	Pin name	Equivalent circuit
14	COMP	
15	FB	
16	REF	

Detailed Description

Power-save Feature

This IC has Power-saving feature to enhance efficiency when the load is light.
By shutting down unnecessary circuits, operating current of the IC is minimized and high efficiency is realized.



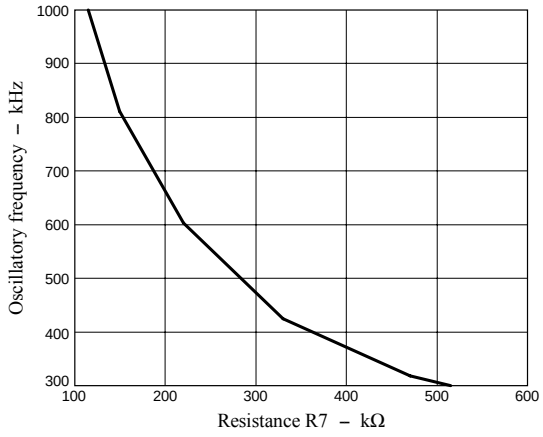
Output Voltage Setting

Output voltage (V_{OUT}) is configurable by the resistance R4 between V_{OUT} and FB and the R5 between FB and GND. V_{OUT} is given by the following equation (1).

$$V_{OUT} = (1 + \frac{R4}{R5}) \times V_{REF} = (1 + \frac{R4}{R5}) \times 1.26 \ [V] \quad (1)$$

Switching Frequency Setting

The switching frequency (F_{OSC}) is set by resistance R7 between RT and GND.
The relation of resistance R7 to switching frequency is shown in a right graph.



Soft Start

Soft start time (T_{SS}) is configurable by the capacitor C7 between SS and GND.
The setting value of T_{SS} is given by the equation (2).

$$T_{SS} = C7 \times \frac{V_{REF}}{I_{SS}} = C7 \times \frac{1.26}{2.0 \times 10^{-6}} \ [ms] \quad (2)$$

Power Good

FB constantly monitors V_{OUT}. When FB voltage is lower than 1.05V, PG is pulled down to Low. PG comparator has hysteresis of 50mV. Because PG is open-drain output, you can connect other ICs with PG to realize wired-or with other ICs.

Hiccup Over-Current Protection

Over current limit (I_{CL}) is set by current sensing resister R1 and resistance (R2) between V_{IN} and I_{LIM}.
The setting value of I_{CL} is given by the equations (3) and (4).

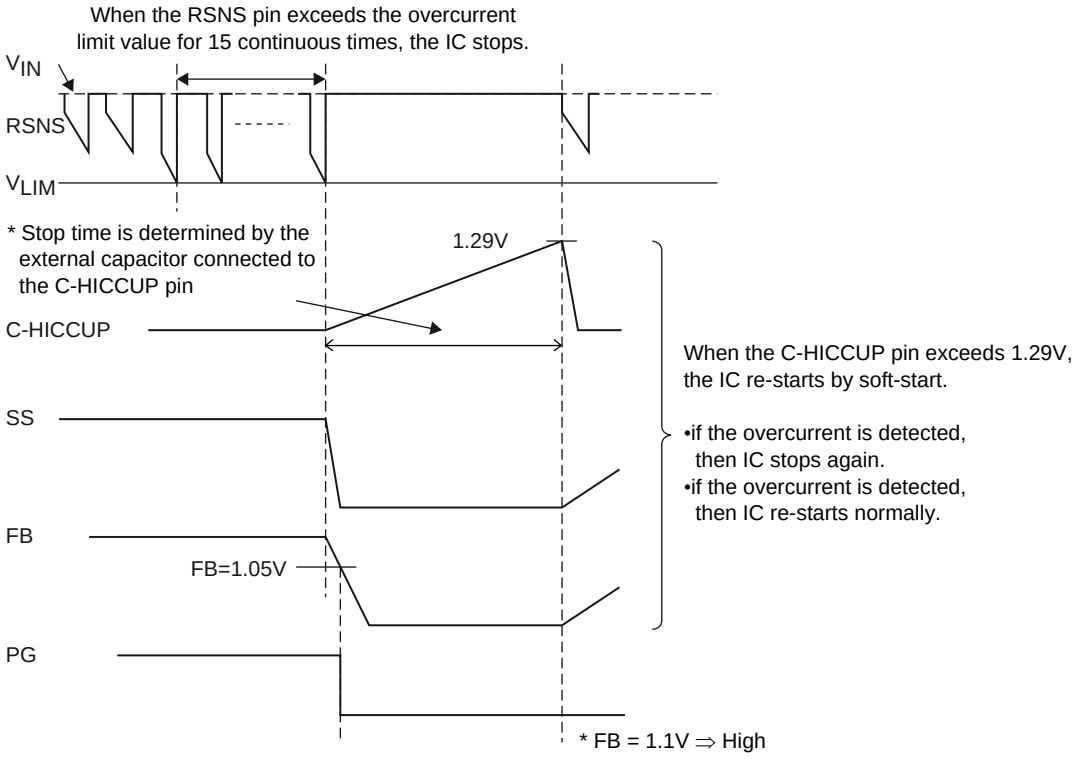
$$V_{LIM} = R2 \times I_{LIM} = R2 \times 55 \times 10^{-6} \ [V] \quad (3)$$

$$I_{CL} = \frac{V_{LIM}}{R1} = \frac{R2 \times 55 \times 10^{-6}}{R1} \ [A] \quad (4)$$

When the voltage between V_{IN} and RSNS (V_{RSNS}) is higher than the voltage between V_{IN} and I_{LIM} for 15 consecutive times, the protection deems it as over current and stops the IC.
Stop period (T_{HIC}) is defined by the external capacitor (C8) of the C-HICCUP.
The setting value of T_{HIC} is given by the equations (5).

$$T_{HIC} = \frac{C8 \times V_{tHIC}}{I_{HIC}} = \frac{C8 \times 1.29}{2.0 \times 10^{-6}} \ [s] \quad (5)$$

When C-HICCUP is about 1.29V, the IC starts up. Regardless of a status; whether it starts up or SS charge, once over current is detected, the IC stops again and when the protection does not detect over current status, the IC starts up again.



Design Procedure

Inductor Selection

When conditions for input voltage, output voltage and ripple current are defined, the following equations (6) give inductance value.

$$\left\{ \begin{array}{l} L = \dfrac{V_{IN} - V_{OUT}}{\Delta I_R} \times T_{ON} \\ T_{ON} = \dfrac{1}{\{((V_{IN} - V_{OUT}) \div (V_{OUT} + VF)) + 1\} \times F_{OSC}} \\ \\ F_{OSC} \quad : \text{Oscillatory Frequency} \\ VF \quad : \text{Forward voltage of Schottky Barrier diode} \\ V_{IN} \quad : \text{Input voltage} \\ V_{OUT} \quad : \text{Output voltage} \end{array} \right. \tag{6}$$

- Inductor current: Peak value (I_{RP})

  Current peak value (I_{RP}) of the inductor is given by the equation (7).

$$I_{RP} = I_{OUT} + \frac{V_{IN} - V_{OUT}}{2L} \times T_{ON} \tag{7}$$

  Make sure that rating current value of the inductor is higher than a peak value of ripple current.

- Inductor current: ripple current (ΔI_R)

  Ripple current (ΔI_R) is given by the equation (8).

$$\Delta I_R = \frac{V_{IN} - V_{OUT}}{L} \times T_{ON} \tag{8}$$

  When load current (I_{OUT}) is less than 1/2 of the ripple current, inductor current flows discontinuously.

Output Capacitor Selection

Make sure to use a capacitor with low impedance for switching power supply because of large ripple current flows through output capacitor.
This IC is a switching regulator which adopts current mode control method. Therefore, you can use capacitor such as ceramic capacitor and OS capacitor in which equivalent series resistance (ESR) is exceedingly small.
Effective value is given by the equation (9) because the ripple current (AC) that flows through output capacitor is saw tooth wave.

$$I_{C\_OUT} = \frac{1}{2\sqrt{3}} \times \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{L \times F_{OSC} \times V_{IN}} \quad [\text{Arms}] \tag{9}$$

Input Capacitor Selection

Ripple current flows through input capacitor which is higher than that of the output capacitors.
Therefore, caution is also required for allowable ripple current value.
The effective value of the ripple current flows through input capacitor is given by the equation (10).

$$I_{C\_IN} = \sqrt{D\,(1 - D)} \times I_{OUT} \quad [\text{Arms}] \tag{10}$$

$$D = \frac{T_{ON}}{T} = \frac{V_{OUT}}{V_{IN}}$$

In (10), D signifies the ratio between ON/OFF period. When the value is 0.5, the ripple current is at a maximum. Make sure that the input capacitor does not exceed the allowable ripple current value given by equation (10).
In the board wiring from input capacitor, V_{IN} to GND, make sure that wiring is wide enough to keep impedance low because of the current fluctuation. Make sure to connect input capacitor near output capacitor to lower voltage bound due to regeneration current. When change of load current is excessive (I_{OUT}: high $\Rightarrow$ low), the power of output electric capacitor is regenerated to input capacitor. If input capacitor is small, input voltage increases. Therefore, you need to implement a large input capacitor. Regeneration power changes according to the change of output voltage, inductance of a coil and load current.

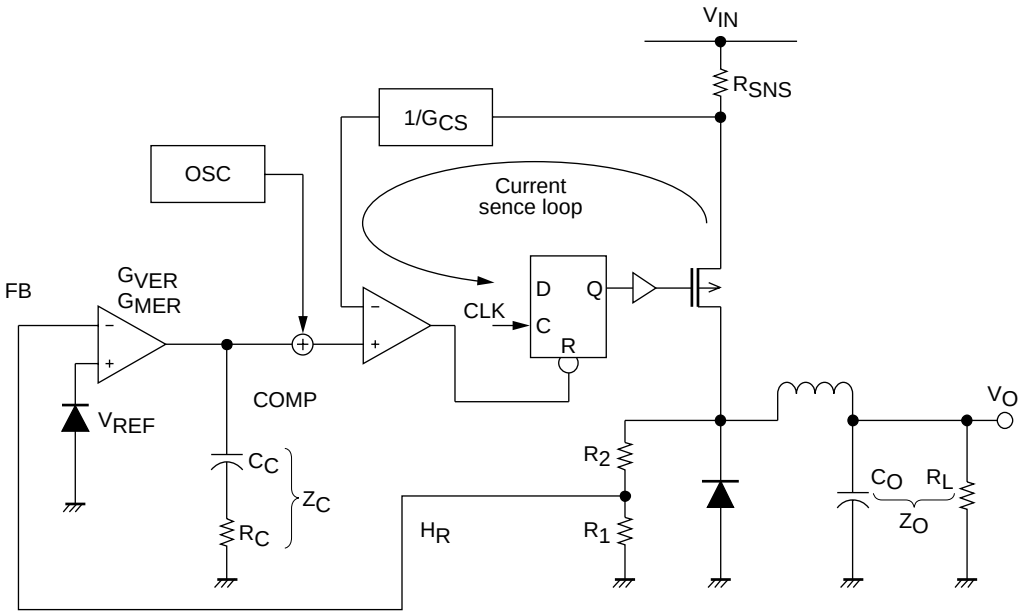
Selection of external phase compensation component

This IC adopts current mode control which allows use of ceramic capacitor with low ESR and solid polymer capacitor such as OS capacitor for output capacitor with simple phase compensation. Therefore, you can design long-life and high quality step-down power supply circuit easily.

Frequency Characteristics

The frequency characteristic of this IC is constituted with the following transfer functions.

(1) Output resistance breeder : H_R
(2) Voltage gain of error amplifier : G_{VEA}
Current gain : G_{MEA}
(3) Impedance of phase compensation external element : Z_C
(4) Current sense loop gain : G_{CS}
(5) Output smoothing impedance : Z_O



Closed loop gain is obtained with the following formula (11).

$$G = H_R \cdot G_{MER} \cdot Z_C \cdot G_{CS} \cdot Z_O$$

$$= \frac{V_{REF}}{V_{OUT}} \cdot G_{MER} \cdot \left(R_C + \frac{1}{SC_C}\right) \cdot G_{CS} \cdot \frac{R_L}{1 + SC_O \cdot R_L} \quad (11)$$

Frequency characteristics of the closed loop gain is given by pole fp1 consists of output capacitor C_O and output load resistance R_L, zero point fz consists of external capacitor C_C of the phase compensation and resistance R_C, and pole fp2 consists of output impedance Z_{ER} of error amplifier and external capacitor of phase compensation C_C as shown in equation (9). fp1, fz, fp2 are obtained with the following equations (12) to (14).

$$fp1 = \frac{1}{2\pi \cdot C_O \cdot R_L} \quad (12)$$

$$fz = \frac{1}{2\pi \cdot C_C \cdot R_C} \quad (13)$$

$$fp2 = \frac{1}{2\pi \cdot Z_{ER} \cdot C_C} \quad (14)$$

Calculation of external phase compensation constant

Generally, to stabilize switching regulator, the frequency where closed loop gain is 1 (zero-cross frequency f_{ZC}) should be $\frac{1}{10}$ of the switching frequency (or $\frac{1}{5}$). Since the switching frequency of this IC is 330kHz, the zero-cross frequency should be 33kHz. Based on the above condition, we obtain the following formula (15).

$$\frac{V_{REF}}{V_{OUT}} \cdot G_{MER} \cdot \left(R_C + \frac{1}{SC_C}\right) \cdot G_{CS} \cdot \frac{R_L}{1 + SC_O \cdot R_L} = 1 \quad (15)$$

As for zero-cross frequency, since the impedance element of phase compensation is $RC >> \frac{1}{SC_C}$, the following equation (16) is obtained.

$$\frac{V_{REF}}{V_{OUT}} \cdot G_{MER} \cdot R_C \cdot G_{CS} \cdot \frac{R_L}{1 + 2\pi \cdot f_{ZC} \cdot C_O \cdot R_L} = 1 \quad (16)$$

Phase compensation external resistance can be obtained with the following equation (16), the variation of the equation (17). Since $2\pi \cdot f_{ZC} \cdot C_O \cdot R_L >> 1$ in the equation (17), we know that the external resistance is independent of load resistance.

$$R_C = \frac{V_{OUT}}{V_{REF}} \cdot \frac{1}{G_{MER}} \cdot \frac{1}{G_{CS}} \cdot \frac{1 + 2\pi \cdot f_{ZC} \cdot C_O \cdot R_L}{R_L} \quad (17)$$

When output is 5V and load resistance is 5Ω (1A load), R_{SNS} is 30mΩ, the resistances of phase compensation are as follows.

$G_{CS} = \frac{0.125}{R_{SNS}} = 4.167A/V$, $G_{MER} = 250\mu A/V$, $f_{ZC} = 33kHz$

$$R_C = \frac{5}{1.26} \times \frac{1}{250 \times 10^{-6}} \times \frac{1}{4.167} \times \frac{1 + 2 \times 3.14 \times (33 \times 10^3) \times (30 \times 10^{-6}) \times 5}{5} = 24.45\ldots \times 10^3$$

$$= 24.45\ [k\Omega]$$

If frequency of zero point fz and pole fp1 are in the same position, they cancel out each other. Therefore, only the pole frequency remains for frequency characteristics of the closed loop gain.
In other words, gain decreases at -20dB/dec and phase only rotates by 90º and this allows characteristics where oscillation never occurs.

$$fp1 = fz$$

$$\frac{1}{2\pi \cdot C_O \cdot R_L} \cdot \frac{1}{2\pi \cdot C_O \cdot R_C}$$

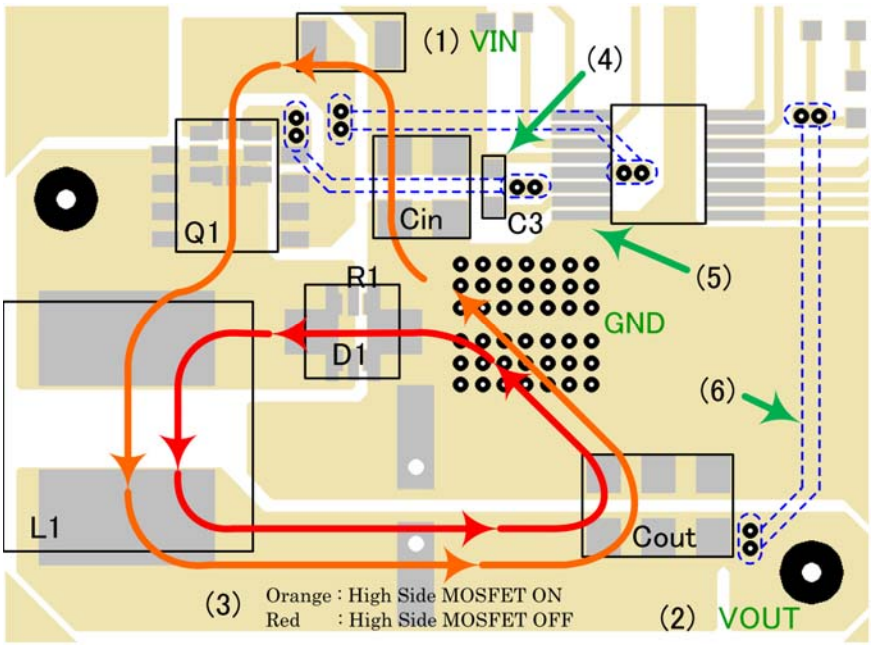
$$C_C = \frac{R_L \cdot C_O}{R_C} \cdot \frac{5 \times (30 \times 10^{-6})}{24.45 \times 10^3} = 6.13\ldots \times 10^{-9}$$

$$= 6.13\ [nF]$$

The above shows external compensation constant obtained through ideal equations. In reality, we need to define phase constant through testing to verify constant IC operation at all temperature range, load range and input voltage range. In the evaluation board for delivery, phase compensation constants are defined based on the above constants. The zero-cross frequency required in the actual system board, in other word, transient response is adjusted by external compensation resistance. Also, if the influence of noise is significant, use of external phase compensation capacitor with higher value is recommended.

Caution in pattern design

Pattern design of the board affects the characteristics of DC-DC converter. This IC switches high current at a high speed. Therefore, if inductance element in a pattern wiring is high, it could be the cause of noise. Make sure that the pattern of the main circuit is wide and short.



(1) Pattern design of the input capacitor

Connect a capacitor near the IC for noise reduction between V_{IN} and the GND. The change of current is at the largest in the pattern between an input capacitor and V_{IN} as well as between GND and an input capacitor among all the main circuits. Hence make sure that the pattern is as thick and short as possible.

(2) Pattern design of an inductor and the output capacitor

High electric current flows into the choke coil and the output capacitor. Therefore this pattern should also be as thick and short as possible.

(3) Pattern design with current channel into consideration

Make sure that when High side MOSFET is ON (red arrow) and OFF (orange arrow), the two current channels runs through the same channel and an area is minimized.

(4) Pattern design of the capacitor between V_{IN}-PDR

Make sure that the pattern of the capacitor between V_{IN} and PDR is as short as possible.

(5) Pattern design of the RSNS

RSNS pattern should also be as think and short as possible for noise reduction.

(6) Pattern design of the small signal GND

The GND of the small signal should be separated from the power GND.

(7) Pattern design of the FB-OUT line

Wire the line shown in red between FB and OUT to the output capacitor as near as possible. When the influence of noise is significant, use of feedback resistors R2 and R3 with lower value is recommended.

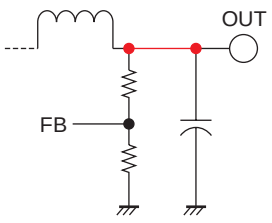
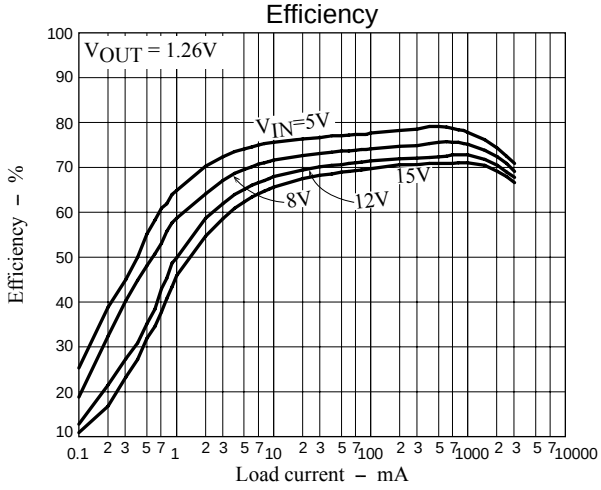


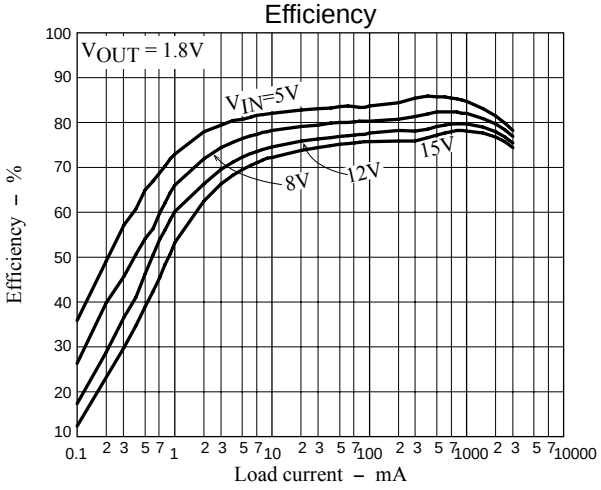
Fig: FB-OUT Line

Typical Performance Characteristics
Application curves at Ta = 25°C

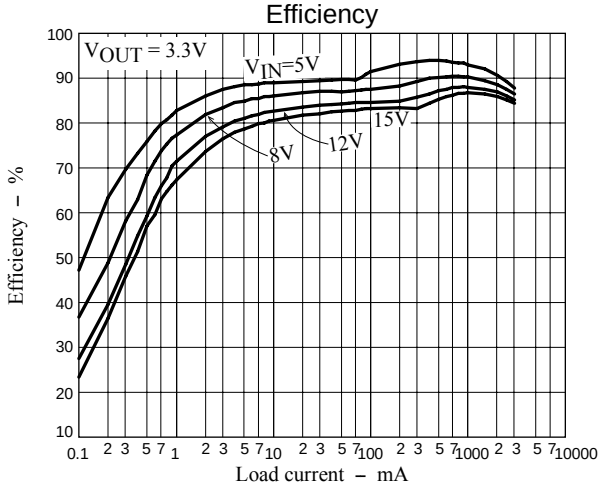
Efficiency



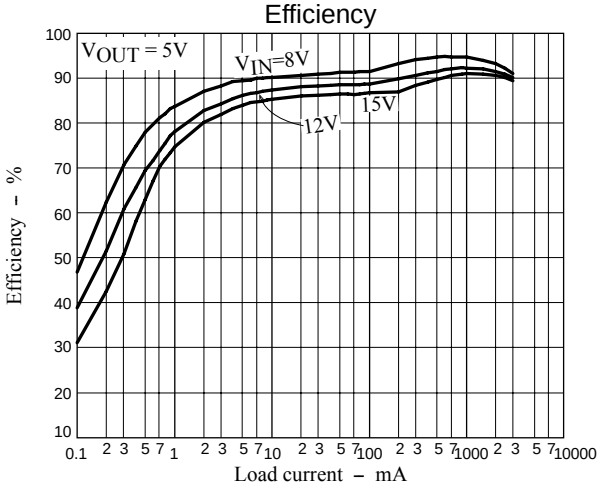
Efficiency



Efficiency

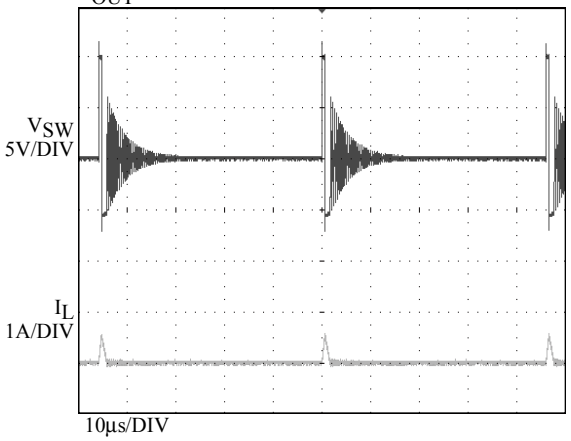


Efficiency

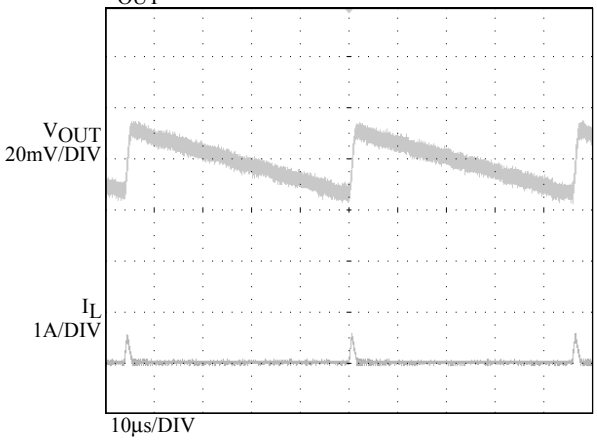


Operation Waveforms (Circuit from Typical Application, Ta = 25°C, V_{IN} = 15V, V_{OUT} = 5V)

Light load mode

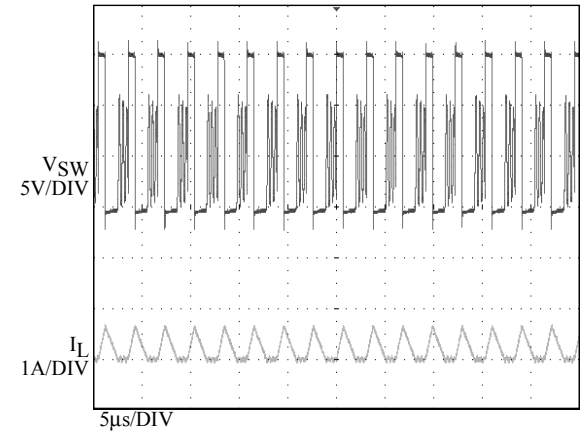


Output Voltage



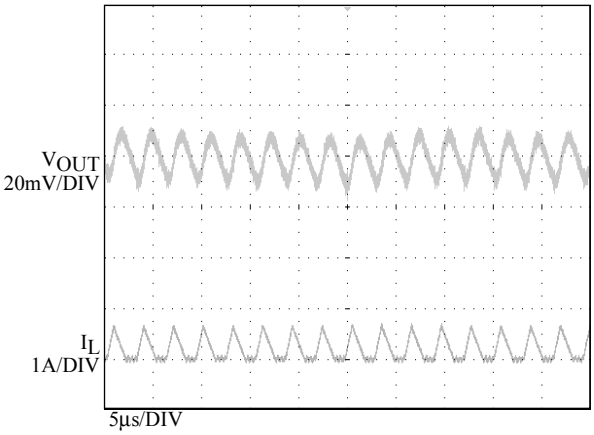
Discontinious current mode

I_{OUT} = 200mA



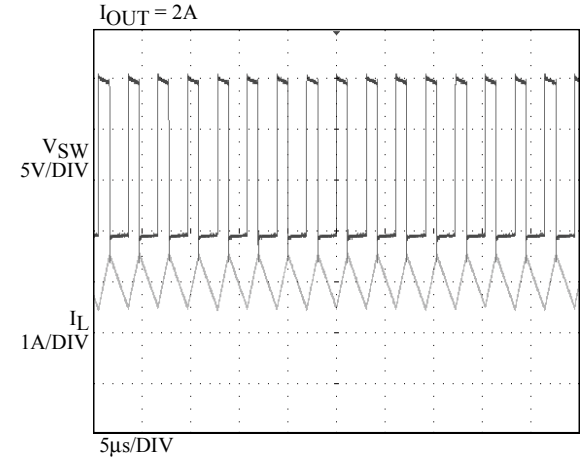
Output Voltage

I_{OUT} = 200mA



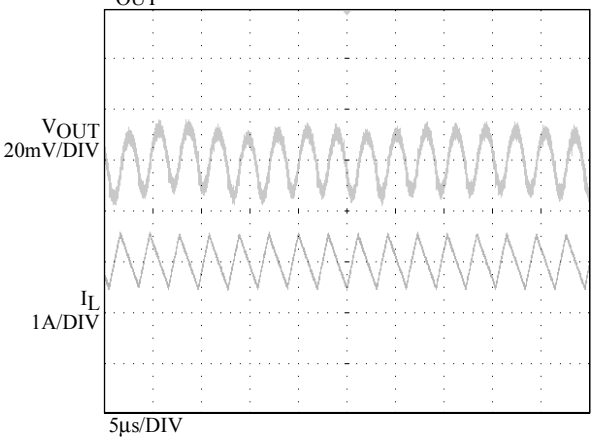
Continious current mode

I_{OUT} = 2A



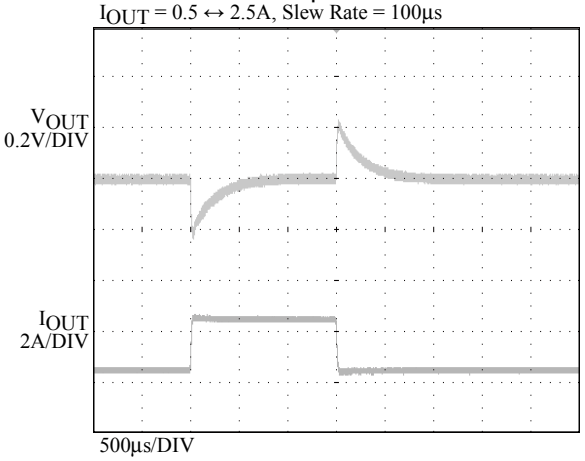
Output Voltage

I_{OUT} = 2A



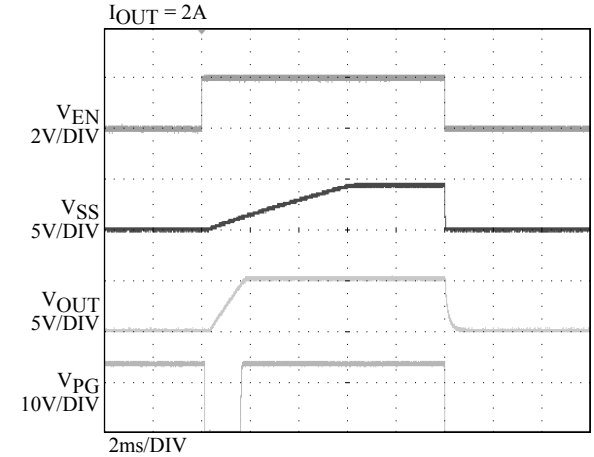
Load Transient response

I_{OUT} = 0.5 ↔ 2.5A, Slew Rate = 100µs



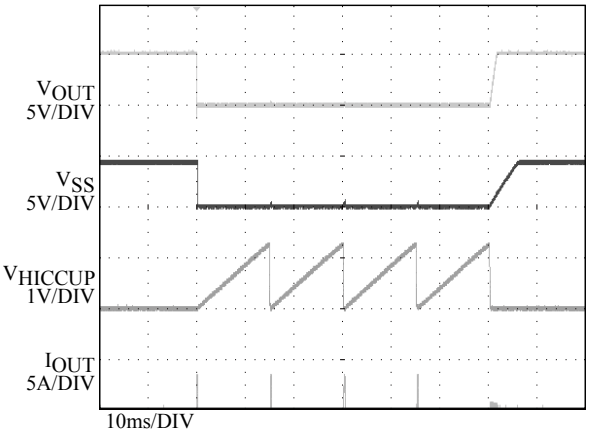
Soft start and shutdown

I_{OUT} = 2A



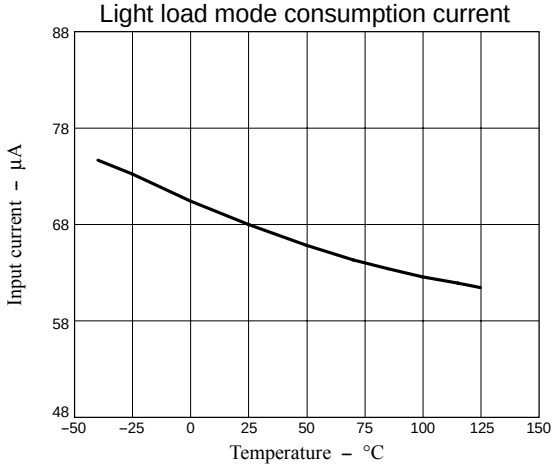
Over current protection

OUT - GND short

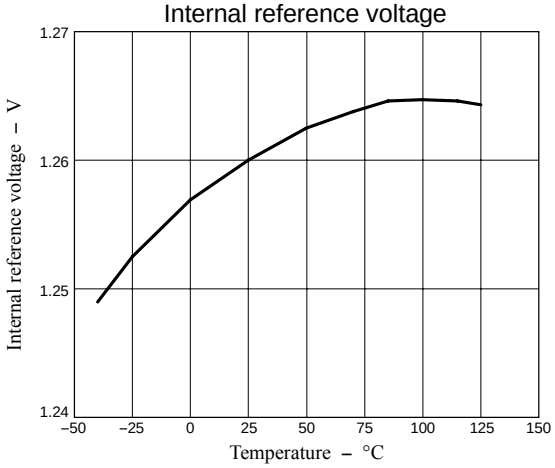


Characterization curves at Ta = 25°C, V_{IN} = 15V

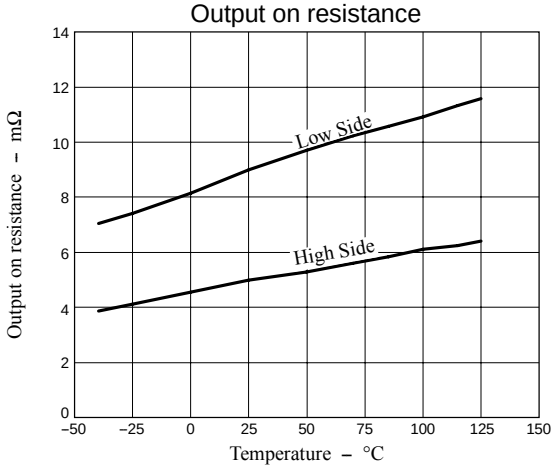
Light load mode consumption current



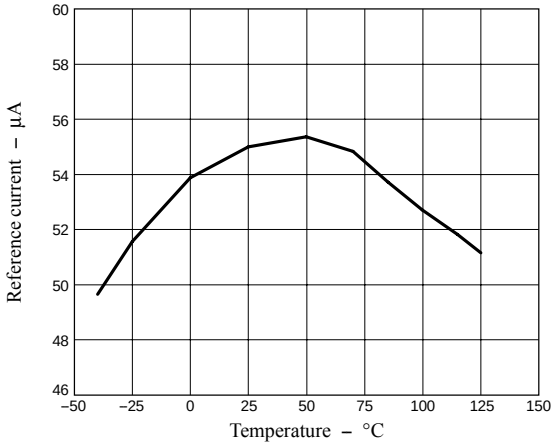
Internal reference voltage



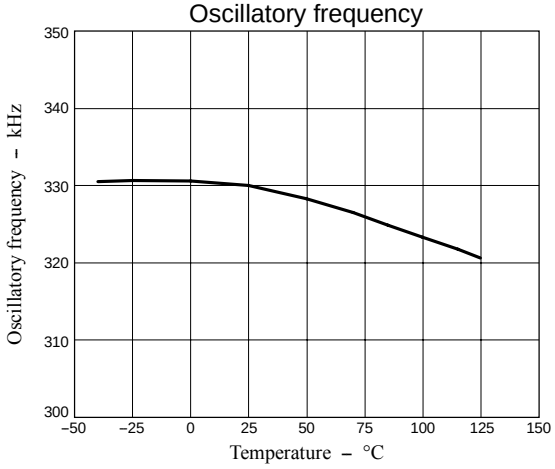
Output on resistance



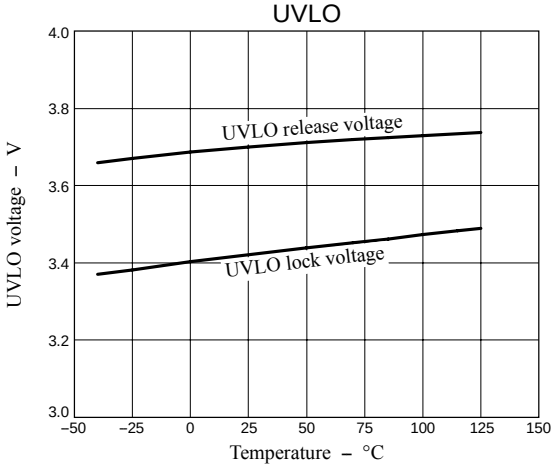
Reference current



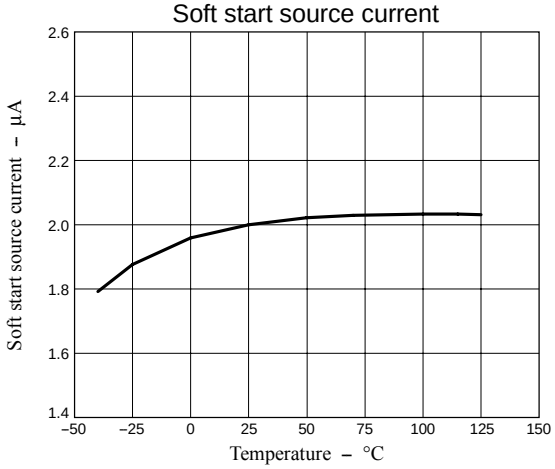
Oscillatory frequency



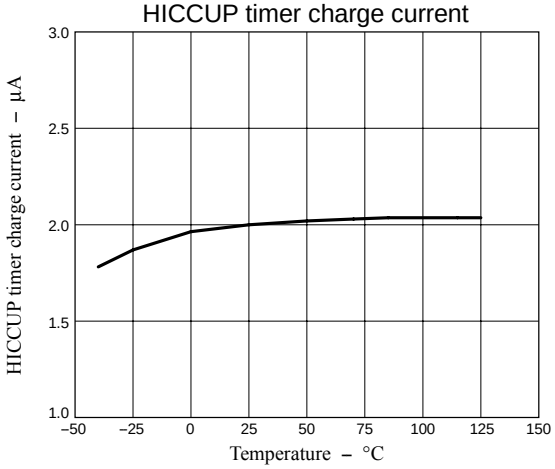
UVLO



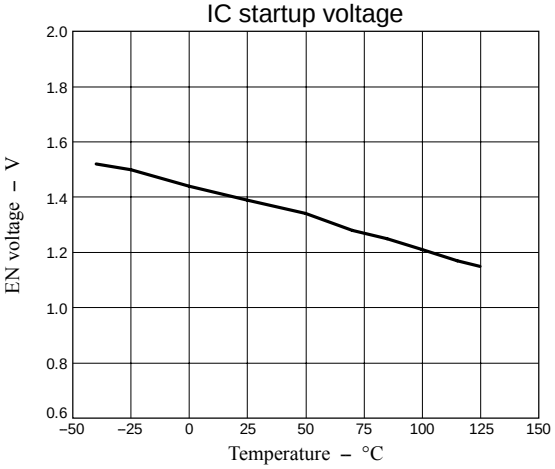
Soft start source current



HICCUP timer charge current



IC startup voltage



Power good threshold voltage