

ISL78692EVAL1Z Evaluation Board User Guide

Description

The ISL78692EVAL1Z is a complete platform for the evaluation on all datasheet specifications and functionalities. The onboard 8-bit DIP switch facilitates battery charge current programming, setting EN input, temperature monitoring status, and so on. The four jumpers can set up input source selection, USB mode selection, and can be used to make other necessary connections.

The ISL78692EVAL1Z board is intended to provide an evaluation platform for the 3mmx3mm DFN ISL78692 package, single-cell Li-ion battery charger.

The device along with key components constitute a complete charger solution, demonstrating the space saving advantage of the ISL78692 in limited space applications.

LEDs connected to STATUS and FAULT pins will indicate the normal charging status or fault condition.

Onboard jumpers and a DIP switch allow the different operating conditions for the charger.

Specifications

- Ambient temperature range, -40°C to +85°C
- Supply voltage, V_{IN} = 4.3V to 5.5V
- Output voltage, VBAT = 4.1V
- · Trickle charge voltage, 2.8V
- · Recharge threshold voltage, 3.9V
- · Constant charge current, 0.5A

Key Features

- · Complete charger for single-cell Li-ion batteries
- · Integrated pass element and current sensor
- · No external blocking diode required
- 1% voltage accuracy
- · Programmable current limit up to 0.5A
- NTC thermistor interface for battery temperature monitor,
 8-bit DIP switch for conveniently setting up charging current,
 battery thermal status, EN input, and so on.
- Different jumpers for input source selection, USB mode selection, and the convenience of current measurement.
- Test points provided for STATUS, FAULT, TIME, EN, V2P8 and TEMP functional pins to allow for monitoring the device pins.
- Board size 3.5" x 2.5" for the convenience of evaluation
- · Eight thermal vias in the thermal pad
- · RoHS compliant

References

• ISL78692 datasheet

Ordering Information

PART #	DESCRIPTION
ISL78692EVAL1Z	Evaluation Board for the 3x3 DFN Package Part



FIGURE 1. TOP VIEW



FIGURE 2. BOTTOM VIEW

What Is Inside

The Evaluation Kit contains:

- ISL78692EVAL1Z board
- The ISL78692 Datasheet
- This ISL78692EVAL1Z User Guide

What Is Needed

The following instruments will be needed to perform testing:

- · Power supplies:
 - PS1: DC 20V/5A,
 - PS2: DC (sinks current) 20V/5A, such as Agilent 6654A
- Electronic load: 20V/5A
- Multimeters
- · Function generator
- Oscilloscope
- · Cables and wires

Quick Setup Guide

Step 1: Switch on bit 4 and bit 7 of the DIP-switch. Leave all other bits off, see Figure 3.

DO NOT APPLY POWER UNTIL STEP 6

- Step 2: Connect 5V to VIN.
- Step 3: Connect 3.7V to VBAT.
- Step 4: Connect 1.2A electronic load to VBAT.
- Step 5: Verify that no shunts are connected across all jumpers.
- Step 6: Turn on Power Supplies and electronic load.
- Step 7: Green LED should be on, indicating normal charging operation.

Step 8: If current meter is in series with VIN, it shall read 400mA as the charging current.

DIP Switch Settings

A 9-bit DIP switch is provided to set up voltage, current reference, end-of-charge (EOC) current, and so on. The functionality of the bits are described in <u>Table 2</u>.

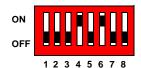


FIGURE 3. INITIAL DIP SWITCH SETTINGS

TABLE 1. JUMPER SETTINGS

JUMPER	POSITION	FUNCTION
	USB TO VIN	USB connection
JP1	WALL CUBE TO VIN	Wall adapter connection
JP2	Installed	Connect VBAT pin to battery Current meter can replace shunt
	Not installed	Default
JP3	Installed	Battery attached to Thermistor at J2
	IREF and V2P8	USB 500mA
JP4	IREF and GND	USB 100mA

TABLE 2. DIP SWITCH PIN DESCRIPTIONS

BIT	DESCRIPTION	ON	OFF	REMARK	
1	Adjustable TIMEOUT	5 hours 50 mins	3 hours 30 mins		
2	Charger enable/disable	Charger disabled	Charger enabled		
3	IREF setting 1	Add 0.5A			
4	IREF setting 2	Add 0.4A			
5				Not connected	
6	TEMP normal	Normal		All off	
7	TEMP high	Too hot		simulates battery	
8	TEMP low	Too cold		removal	

Initial Board Jumper Positioning (Refer to "Schematic" on page 4)

JP1 - Selects the VIN pin connection to a wall adapter, or to USB connector. If J1 connector is being used, a shunt must be installed across JP1-1, 2 or if J3 (USB) connector is being used a shunt must be installed across JP1-2, 3. J1, J3 and JP1 can be ignored if power supply is connected directly to VIN test point, which is directly connected to the VIN pin of the IC. A current meter can replace the shunt mentioned above, so as to measure the input current.

JP2 - Connects the VBAT pin to the battery. If the J2 connector is being used, a shunt must be installed across JP2. A current meter can also replace the shunt to measure the VBAT current.

JP3 - Connects the TEMP pin to the battery. Usually no shunt is needed for JP3, as the evaluation board can simulate various battery thermal conditions. Only when a battery attached with a thermistor is applied on J2 does it become necessary to install a shunt across JP3, and at the same time, bits 6, 7, 8 on the DIP switch all need to be turned off.

JP4 - Selects USB modes: a shunt across IREF and V2P8 will set USB 500mA mode, a shunt across IREF and GND will set USB 100mA mode. When the charge current is programmed by the resistors connected to IREF pin, no shunt should be installed on JP4.

PCB Layout Recommendations

The ISL78692 internal thermal foldback function limits the charge current when the internal temperature reaches approximately +100°C. In order to maximize the current capability, it is very important that the exposed pad under the package is properly soldered to the board and is connected to other layers through thermal vias. More thermal vias and more

copper attached to the exposed pad usually result in better thermal performance. On the other hand, the number of vias is limited by the size of the pad. The 3x3 DFN package allows 9 vias be placed in three rows. Since the pins on the 3x3 DFN package are on only two sides, as much top layer copper as possible should be connected to the exposed pad to minimize the thermal impedance. Refer to "PCB Layout" starting on page 6.

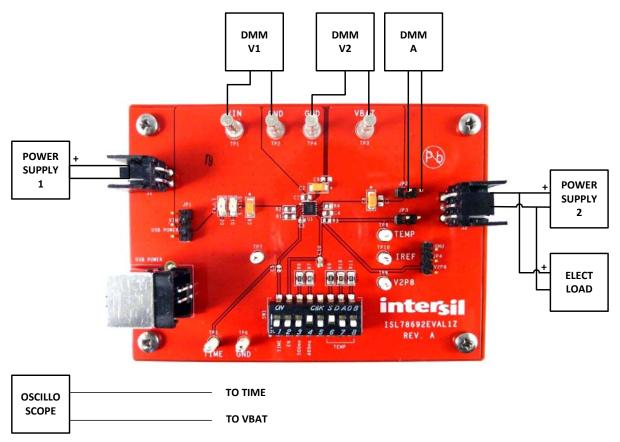


FIGURE 4. CONNECTION OF INSTRUMENTS

Schematic

JP2 **VBAT** OUTPUT C7 OPEN VIN CO COPEN C2 + 10UF C1 GND1 1UF 2 1 ₹ \$8 R4 ONP U1 δ ≶ ξ 2 10 VBAT **TP10** FAULT TEMP FAULT TEMP STATUS **IREF** STATUS IREF TIME V2P8 V2P8 TP5 JP4 ΕN EN TP8 C5 18000PF C3 0.015UF 11 EPAD 2 + ₽ ISL78692-1CR3Z 7 -₹ \$ 200K 87 ₹99. 0.01UF 3 4 SW1 TIME ΕN 500MA JP4 400MA 1,2 USB 500MA NA 2,3 USB 100MA TEMP TEMP TEMP

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Bill of Materials

QTY	UNITS	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER	MANUFACTURER PART NUMBER
1	ea		PWB-PCB, ISL78692EVAL1Z, REVA, ROHS		ISL78692EVAL1ZREVAPCB
2	ea	C1, C4	CAP, SMD, 0603, 1.0µF, 16V, 10%, X7R, ROHS	TDK	C1608X7R1C105K
1	ea	C3	CAP, SMD, 0402, 0.015µF, 16V, 10%, X7R, ROHS	PANASONIC	ECJ-0EB1C153K
1	ea	C 5	CAP, SMD, 0402, 0.018µF, 16V, 10%, X7R, ROHS	MURATA	GRM155R71C183KA01D
1	ea	C10	CAP, SMD, 0603, .01µF, 16V, 10%, X7R, ROHS	VENKEL	C0603X7R160-103KNE
0	ea	C7, C9	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS		
3	ea	C2, C6, C8	CAP-TANT, LOW ESR, SMD, A, 10 μ F, 16V, 20%, 200m Ω , ROHS	AVX	TCJA106M016R0200
4	ea	TP1-TP4	CONN-TURRET, TERMINAL POST, TH, ROHS	KEYSTONE	1514-2
1	ea	J1	CONN-HEADER, 2P, SHROUDED, 2.54mm, RT.ANGLE, ROHS	AMP/TYCO	2-644803-2
1	ea	J2	CONN-HEADER, 3P,SHROUDED, 2.54mm, RT.ANGLE, ROHS	AMP/TYCO	2-644803-3
1	ea	J3	CONN-TYPE B RECEPTACLE, TH,4 POS, RT.ANGLE, ROHS	AMP/TYCO	292304-1
6	ea	TP5-TP10	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	KEYSTONE	5002
2	ea	JP1, JP4	CONN-HEADER, 1x3, BREAKAWY 1X36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
2	ea	JP2, JP3	CONN-HEADER, 1X2, RETENTIVE, 2.54mm, 0.230X 0.120, ROHS"	BERG/FCI	69190-202HLF
1	ea	D2	LED, SMD, 1206, RED, 30mA, 60mW, 17mcd, ROHS	DIALIGHT	597-3111-407F
1	ea	D1	LED, SMD, 1206 ,GREEN, 75mW, 3mcd, Pb- Free	DIALIGHT	597-3311-407F
1	ea	U1	IC-4.1V LI-ION/LI POLYMER CHARGER, 10LD DFN 3X3, ROHS	INTERSIL	ISL78692-1CR3Z
1	ea	R3	RES, SMD, 0402, 10k, 1/16W, 1%, TF, ROHS	PANASONIC	ERJ-2RKF1002X
0	ea	R4	RES, SMD, 0402, DNP, DNP, DNP, TF, ROHS		
2	ea	R1, R2	RES, SMD, 0603, 220Ω, 1/10W, 1%, TF, ROHS	YAGEO	9C06031A2200FKHFT
1	ea	R6	RES, SMD, 0805, 158k, 1/8W, 1%, TF, ROHS	YAGEO	RC0805FR-07158KL
1	ea	R11	RES, SMD, 0805, 18.2k, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-6ENF1822V
1	ea	R7	RES, SMD, 0805, 200k, 1/8W, 1%, TF, ROHS	VENKEL	CR0805-8W-2003FT
1	ea	R10	RES, SMD, 0805, 499Ω, 1/8W, 1%, TF, ROHS	YAGEO	RC0805FR-07499RL
1	ea	R9	RES, SMD, 0805, 4.99k, 1/8W, 1%, TF, ROHS	PANASONIC	ERJ-6ENF4991V
1	ea	SW1	SWITCH-DIP, SMD, 8POS, TOP SLIDE, SPST, 24V, ROHS	C&K COMPONENTS	SDA08H1SBD
4	ea	Four corners	SCREW, 4-40X1/4in, PAN, SS, PHILLIPS		
4	ea	Four corners	STANDOFF, 4-40X3/4in, F/F, HEX, ALUMINUM, ROHS	KEYSTONE	2204 (.250 OD)

PCB Layout

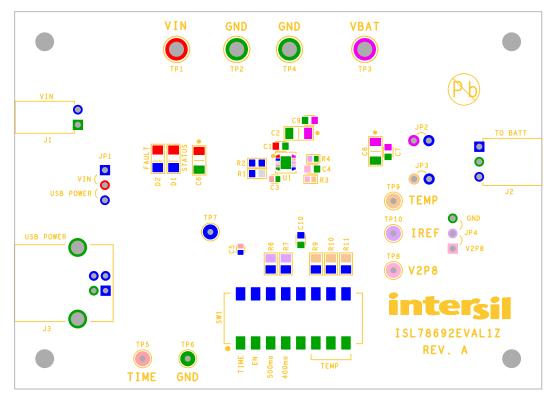


FIGURE 5. SILK LAYER TOP

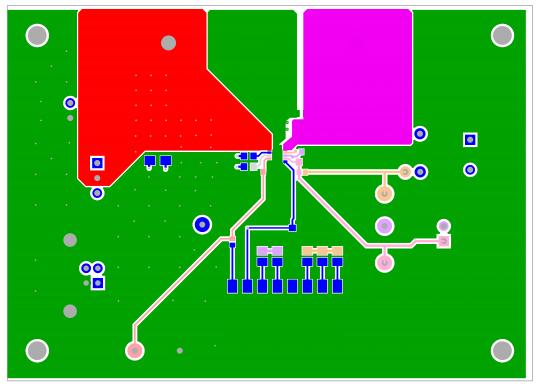


FIGURE 6. TOP LAYER COMPONENT SIDE

PCB Layout (Continued)

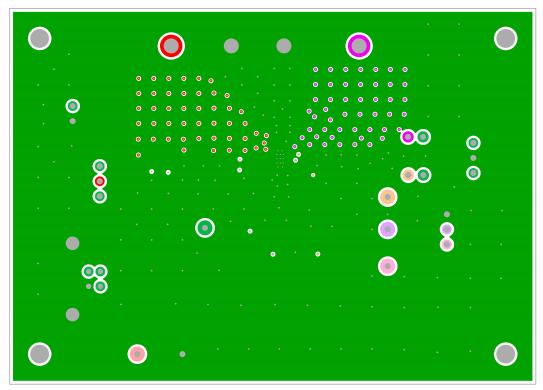


FIGURE 7. INTERNAL (LAYER 2)

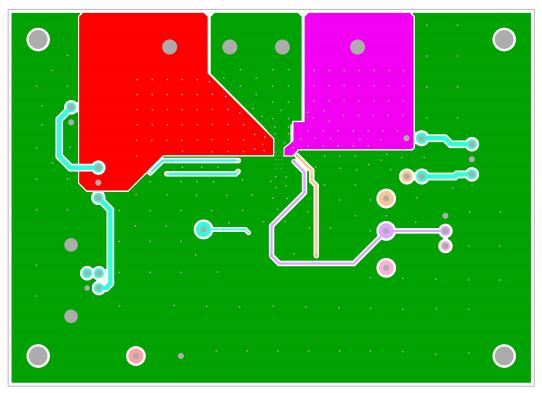


FIGURE 8. INTERNAL (LAYER 3)

PCB Layout (Continued)

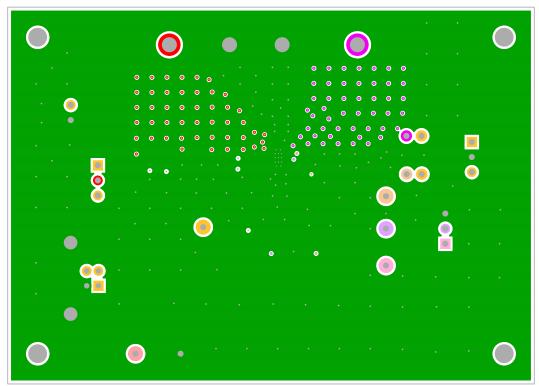


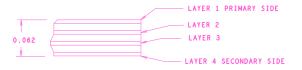
FIGURE 9. BOTTOM LAYER SOLDER SIDE

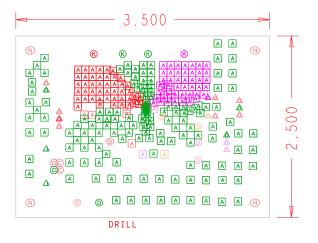


FIGURE 10. SILKSCREEN BOTTOM

06001.0 September 10, 2014

PCB Layout (Continued)





DRILL CHART: TOP to BOTTOM				
	ALL UNITS ARE	IN MILS		
FIGURE	SIZE	PLATED	QTY	
(8)	8.0	PLATED	14	
A	12.0	PLATED	242	
©	37.0	PLATED	4	
0	40.0	PLATED	6	
Δ	41.0	PLATED	15	
Δ	91.0	PLATED	2	
(K)	100.0	PLATED	4	
N	125.0	NON-PLATED	4	

IOTES -

- 1. THIS BOARD IS ROHS COMPLIANT.
- PRINTED WIRING BOARD DESIGN AND ACCEPTANCE CRITERIA SHALL BE IAW WITH THE REQUIREMENTS OF IPC-D-275 AND IPC-A-600.
- 3. MATERIAL: FR4 (RoHS COMPLIANT), 1 OZ COPPER.
- APPLY SOLDER MASK, BOTH SIDES OVER BARE COPPER IAW IPC-SM-840. CLASS 2 (LPI) (INTERSIL RED MASK).
- 5. ALL PATTERNS ARE VIEWED FROM THE PRIMARY SIDE LOOKING THROUGH THE BOARD.
- 6. UNLESS OTHERWISE SPECIFIED ALL HOLE DIAMETERS ARE AFTER PLATING.
- 7. APPLY SILKSCREEN USING WHITE NON-CONDUCTIVE EPOXY BASED INK.
- PWB MUST BE 100% ELECTRICALLY TESTED FOR SHORTS AND CONTINUITY.
 USE NETLIST PROVIDED ISL78691EVAL1ZA_IPC356.IPC IAW IPC-D-356.
- MARK DATE CODE AND MANUFACTURES IDENIFICATION ON SOLDER SIDE PER IPC-6011 AND IPC-6012.
- 10. TOLERANCE ON ALL DRILL HOLES SHALL BE IAW IPC-D-2221 & 2222 UNLESS OTHERWISE SPECIFIED.

FIGURE 11A. PCB AND DRILL SPECIFICATIONS

Typical Performance Curves

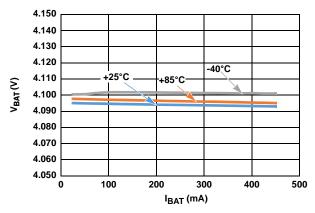


FIGURE 12. VOLTAGE REGULATION vs CHARGE CURRENT

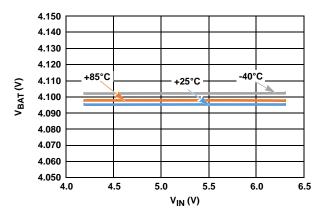


FIGURE 13. NO LOAD VOLTAGE vs TEMPERATURE

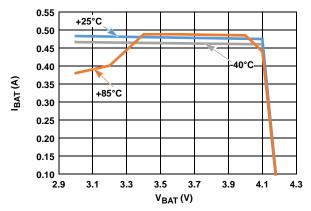


FIGURE 14. CHARGE CURRENT vs OUTPUT VOLTAGE, $R_{IREF} = 158k$

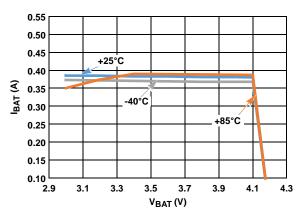


FIGURE 15. CHARGE CURRENT vs OUTPUT VOLTAGE, $R_{IREF} = 200k$

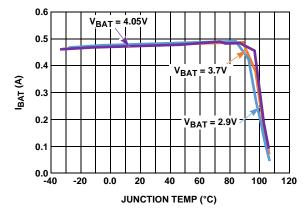


FIGURE 16. CHARGE CURRENT vs JUNCTION TEMPERATURE, $R_{IREF} = 158 k$

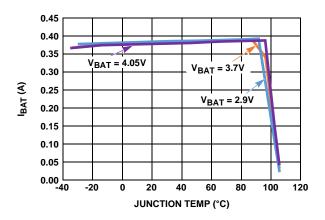


FIGURE 17. CHARGE CURRENT vs JUNCTION TEMPERATURE, RIREF = 200k

Typical Performance Curves

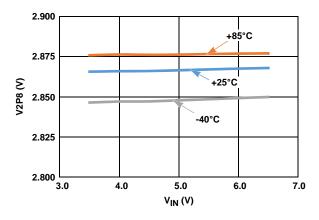


FIGURE 18. V2P8 OUTPUT vs INPUT VOLTAGE AT NO LOAD

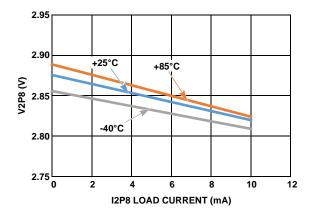


FIGURE 19. V2P8 OUTPUT vs LOAD CURRENT

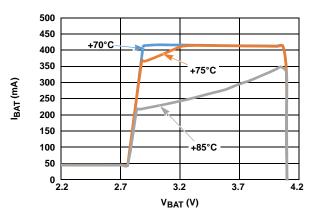


FIGURE 20. V_{BAT} vs I_{BAT} vs AMBIENT TEMPERATURE, R_{IREF} = 200k, V_{IN} = 5.5V, AIR FLOW = 0 LFM, MEASURED ON THE ISL78692EVAL1Z BOARD

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.