ANALOG DEVICES

LC²MOS
(8+4) Loading Dual 12-Bit DAC

AD7937

FEATURES
Two 12-Bit DACs in One Package
DAC Ladder Resistance Matching: 0.5%
Surface-Mount Package
4-Quadrant Multiplication
Low Gain Error (3 LSB max Over Temperature)
Byte Loading Structure
Fast Interface Timing

APPLICATIONS
Automatic Test Equipment
Programmable Filters
Audio Applications
**Synchro Applications**
Process Control

GENERAL DESCRIPTION

The AD7937 contains two 12-bit current output DACs on one monolithic chip. A separate reference input is provided for each DAC. The dual DAC saves valuable board space, and the monolithic construction ensures excellent thermal tracking. Both DACs are guaranteed 12-bit monotonic over the full temperature range.

The AD7937 has a 2-byte (eight LSBs, four MSBs) loading structure. It is designed for right-justified data format. The control signals for register loading are A0, A1, $\overline{CS}$, $\overline{WR}$, and $\overline{UPD}$. Data is loaded to the input registers when $\overline{CS}$ and $\overline{WR}$ are low. To transfer this data to the DAC registers, $\overline{UPD}$ must be taken low with $\overline{WR}$.

Added features on the AD7937 include an asynchronous $\overline{CLR}$ line which is very useful in calibration routines. When this is taken low, all registers are cleared. The double buffering of the data inputs allows simultaneous update of both DACs. Also, each DAC has a separate AGND line. This increases the device versatility; for instance, one DAC may be operated with AGND biased while the other is connected in the standard configuration.

The AD7937 is manufactured using the Linear Compatible CMOS (LC²MOS) process. It is speed compatible with most microprocessors and accepts TTL, 74HC, and 5 V CMOS logic level inputs.

FUNCTIONAL BLOCK DIAGRAM
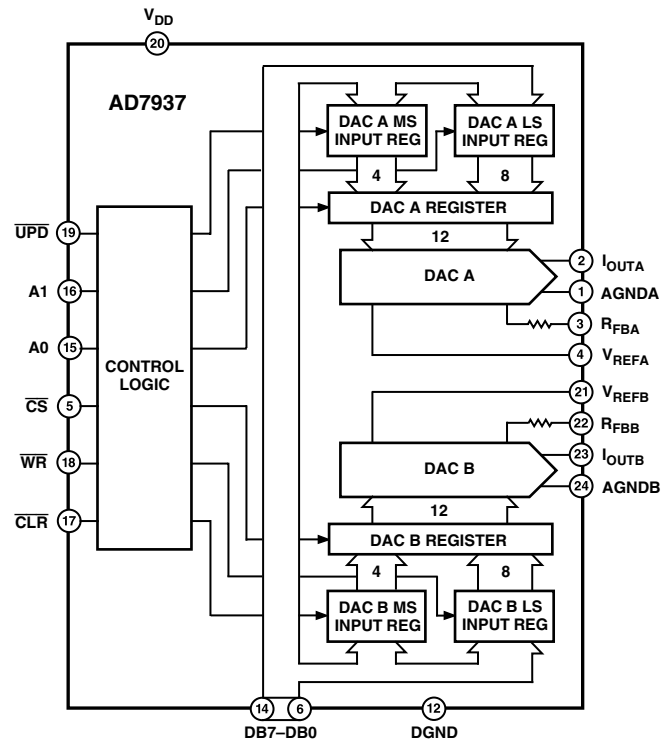
PRODUCT HIGHLIGHTS

1. DAC-to-DAC Matching
   Since both DACs are fabricated on the same chip, precise matching and tracking is inherent. Many applications that are not practical using two discrete DACs are now possible. Typical matching: 0.5%.

2. Small Package Size
   The AD7937 is packaged in a small 24-lead SOIC.

3. Wide Power Supply Tolerance
   The device operates on a 5 V V_{DD}, with ±10% tolerance on this nominal figure. All specifications are guaranteed over this range.

REV. 0

AD7937–SPECIFICATIONS

(V_{DD} = 5 V ± 10%, V_{REFA} = V_{REFB} = 10 V; I_{OUTA} = AGNDA = 0 V, I_{OUTB} = AGNDB = 0 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Version	B Version	Unit	Test Conditions/Comments
ACCURACY				
Resolution	12	12	Bits	
Relative Accuracy	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	All grades guaranteed monotonic over temperature.
Gain Error	±6	±3	LSB max	Measured using R_{FBA}, R_{FBB}. Both DAC registers loaded with all 1s.
Gain Temperature Coefficient[2];				
ΔGain/ΔTemperature	±5	±5	ppm/°C max	Typical value is 1 ppm/°C.
Output Leakage Current				
I_{OUTA}	5	5	nA max	DAC A Register loaded with all 0s.
	10	10	nA max	
I_{OUTB}	5	5	nA max	DAC B Register loaded with all 0s.
	10	10	nA max	
REFERENCE INPUT				
Input Resistance	9	9	kΩ min	Typical Input Resistance = 14 kΩ.
	20	20	kΩ max	
V_{REFA}, V_{REFB}				
Input Resistance Match	±3	±3	% max	Typically ±0.5%.
DIGITAL INPUTS				
V_{IH} (Input High Voltage)	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	V max	
I_{IN} (Input Current)				
+25°C	±1	±1	µA max	V_{IN} = V_{DD}.
T_{MIN} to T_{MAX}	±10	±10	µA max	
C_{IN} (Input Capacitance)[2]	10	10	pF max	
POWER SUPPLY				
V_{DD}	4.5/5.5	4.5/5.5	V min/V max	
I_{DD}	2	2	mA max	
	0.1	0.1	mA typ	

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.

(V_{DD} = 5 V; V_{REFA} = V_{REFB} = 10 V; I_{OUTA} = AGNDA = 0 V, I_{OUTB} = AGNDB = 0 V. Output Amplifiers are AD644 except where noted.)

Parameter	T_A = 25°C	Unit	Test Conditions/Comments
Output Current Settling Time	1	µs max	To 0.01% of full-scale range. I_{OUT} load = 100 Ω, C_{EXT} = 13 pF. DAC output measured from falling edge of $\overline{WR}$. Typical Value of Settling Time is 0.6 µs.
Digital-to-Analog Glitch Impulse	2.5	nV-s typ	Measured with V_{REFA} = V_{REFB} = 0 V. I_{OUTA}, I_{OUTB} load = 100 Ω, C_{EXT} = 13 pF. DAC registers alternately loaded with all 0s and all 1s.
AC Feedthrough			
V_{REFA} to I_{OUTA}	−70	dB max	V_{REFA}, V_{REFB} = 20 V p-p 10 kHz sine wave.
V_{REFB} to I_{OUTB}	−70	dB max	DAC registers loaded with all 0s.
Power Supply Rejection			
ΔGain/ΔV_{DD}	±0.01	% per % max	ΔV_{DD} = V_{DD} max − V_{DD} min.
Output Capacitance			
C_{OUTA}	70	pF max	DAC A, DAC B loaded with all 0s.
C_{OUTB}	70	pF max	
C_{OUTA}	140	pF max	DAC A, DAC B loaded with all 1s.
C_{OUTB}	140	pF max	
Channel-to-Channel Isolation			
V_{REFA} to I_{OUTB}	−84	dB typ	V_{REFA} = 20 V p-p 10 kHz sine wave, V_{REFB} = 0 V. Both DACs loaded with all 1s.
V_{REFB} to I_{OUTA}	−84	dB typ	V_{REFB} = 20 V p-p 10 kHz sine wave, V_{REFA} = 0 V. Both DACs loaded with all 1s.
Digital Crosstalk	2.5	nV-s typ	Measured for a Code Transition of all 0s to all 1s. I_{OUTA}, I_{OUTB} load = 100 Ω, C_{EXT} = 13 pF.
Output Noise Voltage Density (10 Hz–100 kHz)	25	nV/√Hz typ	Measured between R_{FBA} and I_{OUTA} or R_{FBB} and I_{OUTB}. Frequency of measurement is 10 Hz–100 kHz.
Total Harmonic Distortion	−82	dB typ	V_{IN} = 6 V rms, 1 kHz. Both DACs loaded with all 1s.

NOTES

[1]Temperature range as follows: A, B Versions: −40°C to +85°C.

[2]Sample tested at 25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS (V_{DD} = 5 V ± 10%, V_{REFA} = V_{REFB} = 10 V; I_{OUTA} = AGNDA = 0 V, I_{OUTB} = AGNDB = 0 V.)

| Parameter	Limit at T_A = 25°C	Limit at T_A = –40°C to +85°C	Unit	Test Conditions/Comments
t_1	10	10	ns min	Address Valid to Write Setup Time
t_2	10	10	ns min	Address Valid to Write Hold Time
t_3	20	40	ns min	Data Setup Time
t_4	30	30	ns min	Data Hold Time
t_5	0	0	ns min	Chip Select or Update to Write Setup Time
t_6	0	0	ns min	Chip Select or Update to Write Hold Time
t_7	115	125	ns min	Write Pulsewidth
t_8	90	100	ns min	Clear Pulsewidth

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*
(T_A = 25°C unless otherwise noted)

V_{DD} to DGND . . . . –0.3 V, +17 V
V_{REFA}, V_{REFB} to AGNDA, AGNDB . . . . ±25 V
V_{RFBA}, V_{RFBB} to AGNDA, AGNDB . . . . ±25 V
Digital Input Voltage to DGND . . . . –0.3 V, V_{DD} +0.3 V
I_{OUTA}, I_{OUTB} to DGND . . . . –0.3 V, V_{DD} +0.3 V
AGNDA, AGNDB to DGND . . . . –0.3 V, V_{DD} +0.3 V
SOIC Package
  θ_{JA}, Thermal Impedance . . . . 72°C/W
Lead Temperature (Soldering, 10 sec) . . . . 300°C
IR Ref Low Peak Temperature . . . . 220°C
Operating Temperature Range
  Industrial (A, B Versions) . . . . –40°C to +85°C
  Storage Temperature . . . . –65°C to +150°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
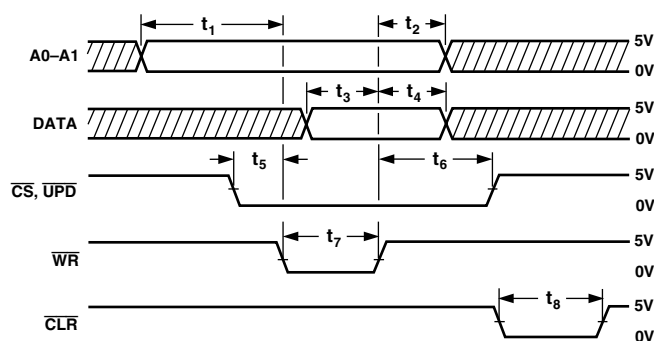
NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. t_r = t_f = 20ns.
2. TIMING MEASUREMENT REFERENCE LEVELS IS $\frac{V_{IH} + V_{IL}}{2}$

Figure 1. Timing Diagram

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Gain Error	Package Description	Option
AD7937AR	–40°C to +85°C	±1 LSB	±6 LSB	Small Outline	R-24
AD7937BR	–40°C to +85°C	±1/2 LSB	±3 LSB	Small Outline	R-24

CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7937 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.
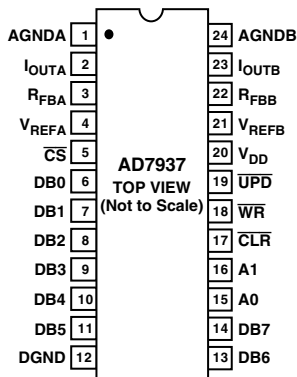
WARNING!
ESD SENSITIVE DEVICE

AD7937

PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Description
1	AGNDA	Analog Ground for DAC A.
2	I_{OUTA}	Current output terminal of DAC A.
3	R_{FBA}	Feedback resistor for DAC A.
4	V_{REFA}	Reference input to DAC A.
5	$\overline{CS}$	Chip Select Input Active low.
6–11 13, 14	DB0–DB7	Eight data inputs, DB0–DB7.
12	DGND	Digital Ground.
15	A0	Address Line 0.
16	A1	Address Line 1.
17	$\overline{CLR}$	Clear Input. Active low. Clears all registers.
18	$\overline{WR}$	Write Input. Active low.
19	$\overline{UPD}$	Updates DAC Registers from inputs registers.
20	V_{DD}	Power supply input. Nominally 5 V to 15 V, with ±10% tolerance.
21	V_{REFB}	Reference input to DAC B.
22	R_{FBB}	Feedback resistor for DAC B.
23	I_{OUTB}	Current output terminal of DAC B.
24	AGNDB	Analog Ground for DAC B.

PIN CONFIGURATION
SOIC

```
         AGNDA  1 ●        24  AGNDB
         I_OUTA 2           23  I_OUTB
         R_FBA  3           22  R_FBB
         V_REFA 4           21  V_REFB
           CS   5   AD7937  20  V_DD
         DB0    6   TOP VIEW 19  UPD
         DB1    7 (Not to Scale) 18  WR
         DB2    8           17  CLR
         DB3    9           16  A1
         DB4   10           15  A0
         DB5   11           14  DB7
         DGND  12           13  DB6
```

CIRCUIT INFORMATION – D/A SECTION

The AD7937 contains two identical 12-bit multiplying D/A converters. Each DAC consists of a highly stable R-2R ladder and 12 N-channel current steering switches. Figure 2 shows a simplified D/A circuit for DAC A. In the R-2R ladder, binary weighted currents are steered between I_{OUTA} and AGNDA. The current flowing in each ladder leg is constant, irrespective of switch state. The feedback resistor R_{FBA} is used with an op amp (see Figures 4 and 5) to convert the current flowing in I_{OUTA} to a voltage output.
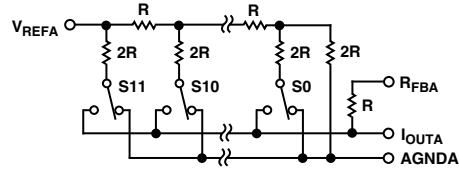

Figure 2. Simplified Circuit Diagram for DAC A

EQUIVALENT CIRCUIT ANALYSIS

Figure 3 shows the equivalent circuit for one of the D/A converters (DAC A) in the AD7937. A similar equivalent circuit can be drawn for DAC B.
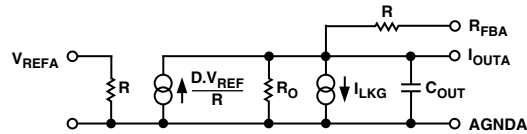

Figure 3. Equivalent Analog Circuit for DAC A

C_{OUT} is the output capacitance due to the N-channel switches and varies from about 50 pF to 100 pF with digital input code. The current source I_{LKG} is composed of surface and junction leakages and approximately doubles every 10°C. R_O is the equivalent output resistance of the device which varies with input code.

DIGITAL CIRCUIT INFORMATION

The digital inputs are designed to be both TTL and 5 V CMOS compatible. All logic inputs are static protected MOS gates with typical input currents of less than 1 nA.

Table I. AD7937 Truth Table

$\overline{CLR}$	$\overline{UPD}$	$\overline{CS}$	$\overline{WR}$	A1	A0	Function
1	1	1	X	X	X	No Data Transfer
1	1	X	1	X	X	No Data Transfer
0	X	X	X	X	X	All Registers Cleared
1	1	0	0	0	0	DAC A LS Input Register Loaded with DB7–DB0 (LSB)
1	1	0	0	0	1	DAC A MS Input Register Loaded with DB3 (MSB)–DB0
1	1	0	0	1	0	DAC B LS Input Register Loaded with DB7–DB0 (LSB)
1	1	0	0	1	1	DAC B MS Input Register Loaded with DB3 (MSB)–DB0
1	0	1	0	X	X	DAC A, DAC B Registers Updated Simultaneously from Input Registers
1	0	0	0	X	X	DAC A, DAC B Registers are Transparent

NOTE: X = Don't care

UNIPOLAR BINARY OPERATION
(2-QUADRANT MULTIPLICATION)

Figure 4 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2-quadrant multiplication. The code table for Figure 4 is given in Table II.

Operational amplifiers A1 and A2 can be in a single package (AD644, AD712) or separate packages (AD544, AD711, AD OP27). Capacitors C1 and C2 provide phase compensation to help prevent overshoot and ringing when high-speed op amps are used.

For zero offset adjustment, the appropriate DAC register is loaded with all 0s and amplifier offset adjusted so that V_{OUTA} or V_{OUTB} is 0 V. Full-scale trimming is accomplished by loading the DAC register with all 1s and adjusting R1 (R3) so that V_{OUTA} (V_{OUTB}) = $-V_{IN}$ (4095/4096). For high temperature operation, resistors and potentiometers should have a low Temperature Coefficient. In many applications, because of the excellent Gain T.C. and Gain Error specifications of the AD7937, Gain Error trimming is not necessary. In fixed reference applications, full scale can also be adjusted by omitting R1, R2, R3, R4 and trimming the reference voltage magnitude.
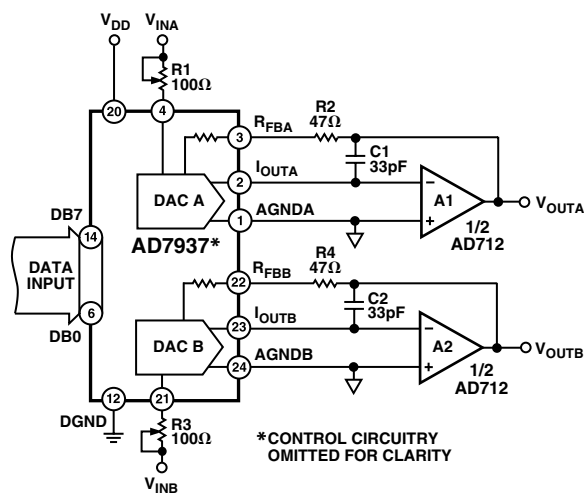

Figure 4. Unipolar Binary Operation

Table II. Unipolar Binary Code Table for Circuit of Figure 4

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUTA} or V_{OUTB}
1111 1111 1111	$-V_{IN}\left(\dfrac{4095}{4096}\right)$
1000 0000 0000	$-V_{IN}\left(\dfrac{2048}{4096}\right)=-\frac{1}{2}V_{IN}$
0000 0000 0001	$-V_{IN}\left(\dfrac{1}{4096}\right)$
0000 0000 0000	$0\ V$

BIPOLAR OPERATION
(4-QUADRANT MULTIPLICATION)

The recommended circuit diagram for bipolar operation is shown in Figure 5. Offset binary coding is used.

With the appropriate DAC register loaded to 1000 0000 0000, adjust R1 (R3) so that V_{OUTA} (V_{OUTB}) = 0 V. Alternatively, R1, R2 (R3, R4) may be omitted and the ratios of R6, R7 (R9, R10) varied for V_{OUTA} (V_{OUTB}) = 0 V. Full-scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R5 (R8).

If R1, R2 (R3, R4) are not used, then resistors R5, R6, R7 (R8, R9, R10) should be ratio matched to 0.01% to ensure gain error performance to the data sheet specification. When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficients match.

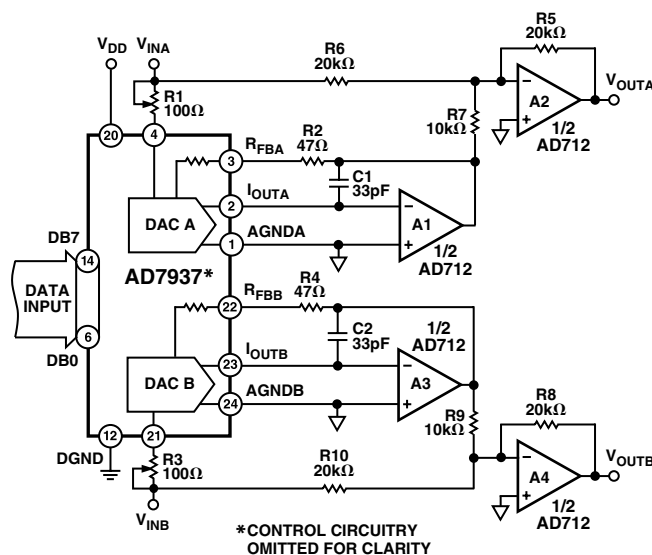The code table for Figure 5 is given in Table III.

Figure 5. Bipolar Operation (Offset Binary Coding)

Table III. Bipolar Code Table for Offset Binary Circuit of Figure 5

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUTA} or V_{OUTB}
1111 1111 1111	$+V_{IN}\left(\dfrac{2047}{2048}\right)$
1000 0000 0001	$+V_{IN}\left(\dfrac{1}{2048}\right)$
1000 0000 0000	$0\ V$
0111 1111 1111	$-V_{IN}\left(\dfrac{1}{2048}\right)$
0000 0000 0000	$-V_{IN}\left(\dfrac{2048}{2048}\right)=-V_{IN}$

AD7937

SEPARATE AGND PINS

The DACs in the AD7937 have separate AGND lines taken to pins AGNDA and AGNDB on the package. This increases the applications versatility of the part. Figure 6 is an example of this. DAC A is connected in standard fashion as a programmable attenuator. AGNDA is at ground potential. DAC B is operating with AGND B biased to 5 V by the AD584. This gives an output range of 5 V to 10 V.
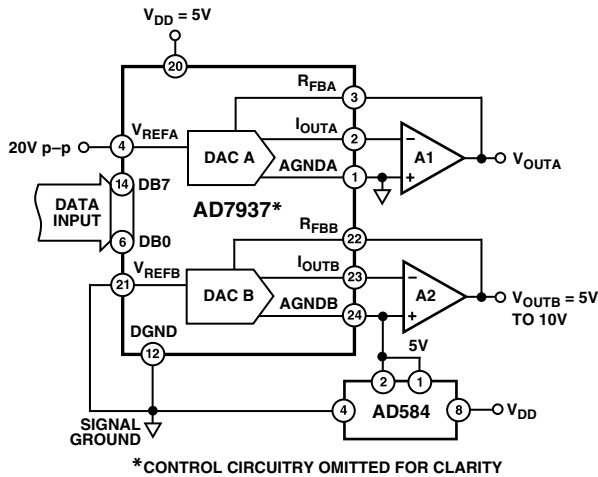

CONTROL CIRCUITRY OMITTED FOR CLARITY

Figure 6. DACs Used in Different Modes

PROGRAMMABLE OSCILLATOR

Figure 7 shows a conventional state variable oscillator in which the AD7937 controls the programmable integrators. The frequency of oscillation is given by:

$$f = \frac{1}{2\pi}\sqrt{\frac{R6}{R5} \times \frac{1}{C1 \times C2 \times R_{EQ1} \times R_{EQ2}}}$$

where R_{EQ1} and R_{EQ2} are the equivalent resistances of the DACs. The same digital code is loaded into both DACs. If $C1 = C2$ and $R5 = R6$, the expression reduces to

$$f = \frac{1}{2\pi} \times \frac{1}{C}\sqrt{\frac{1}{R_{EQ1} \times R_{EQ2}}}$$

Since $R_{EQ} = \dfrac{2^n \times R_{LAD}}{N}$, ($R_{LAD}$ = DAC ladder resistance).

$$f = \frac{1}{2\pi} \times \frac{1}{C}\sqrt{\frac{(N/2^n)^2}{R_{LAD1} \times R_{LAD2}}}$$

$$= \frac{1}{2\pi} \times \frac{D}{C}\frac{1}{\sqrt{R_{LAD1} \times R_{LAD2}}} \quad D = \left(\frac{N}{2^n}\right)$$

$$= \frac{1}{2\pi} \times \frac{D}{C \times R_{LAD}\sqrt{m}}$$

where m is the DAC ladder resistance mismatch ratio, typically 1.005.

With the values shown in Figure 7, the output frequency varies from 0 Hz to 1.38 kHz. The amplitude of the output signal at the A3 output is 10 V peak-to-peak and is constant over the entire frequency span.
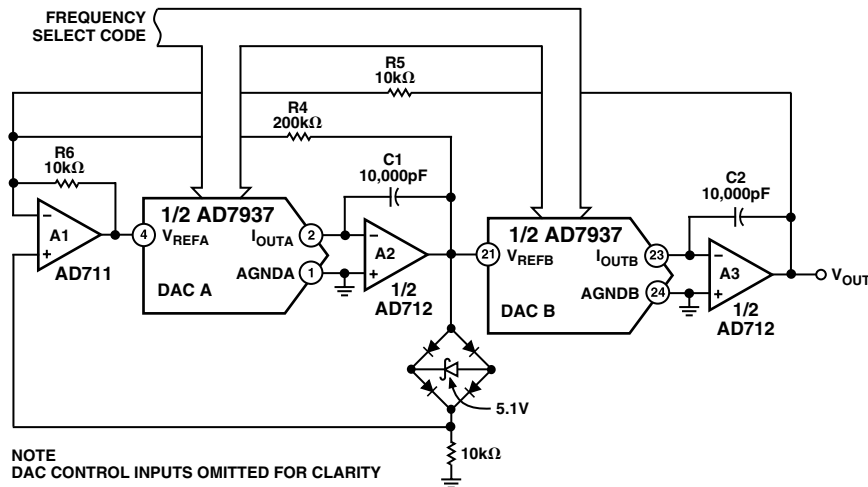

NOTE
DAC CONTROL INPUTS OMITTED FOR CLARITY

Figure 7. Programmable State Variable Oscillator

APPLICATION HINTS

Output Offset: CMOS D/A converters in circuits such as Figures 4 and 5 exhibit a code-dependent output resistance which in turn can cause a code-dependent error voltage at the output of the amplifier. The maximum amplitude of this error, which adds to the D/A converter nonlinearity, depends on V_{OS}, where V_{OS} is the amplifier input offset voltage. To maintain specified operation, it is recommended that V_{OS} be no greater than (25×10^{-6}) (V_{REF}) over the temperature range of operation. Suitable op amps are the AD711C and its dual version, the AD712C. These op amps have a wide bandwidth and high slew rate and are recommended for wide bandwidth ac applications. AD711/AD712 settling time to 0.01% is typically 3 μs.

Temperature Coefficients: The gain temperature coefficient of the AD7937 has a maximum value of 5 ppm/°C and typical value of 1 ppm/°C. This corresponds to worst case gain shifts of 2 LSBs and 0.4 LSBs respectively over a 100°C temperature range. When trim resistors R1 (R3) and R2 (R4) are used to adjust full scale range as in Figure 4, the temperature coefficient of R1 (R3) and R2 (R4) should also be taken into account.

High Frequency Considerations: AD7937 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open-loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor. This is shown as C1 and C2 in Figures 4 and 5.

Feedthrough: The dynamic performance of the AD7937 depends upon the gain and phase stability of the output amplifier, together with the optimum choice of PC board layout and decoupling components.

MICROPROCESSOR INTERFACING

The byte loading structure of the AD7937 makes it very easy to interface the device to any 8-bit microprocessor system. Figure 8 shows an example 8-bit interface between the AD7937 and a generic 8-bit microcontroller/DSP processor. Pins D7 to D0 of the processor are connected to pins D7 to D0 of the AD7937. When writing to the DACs, the lower 8 bits must be written first, followed by the upper four bits. The upper four bits should be output on data lines D0 to D3.
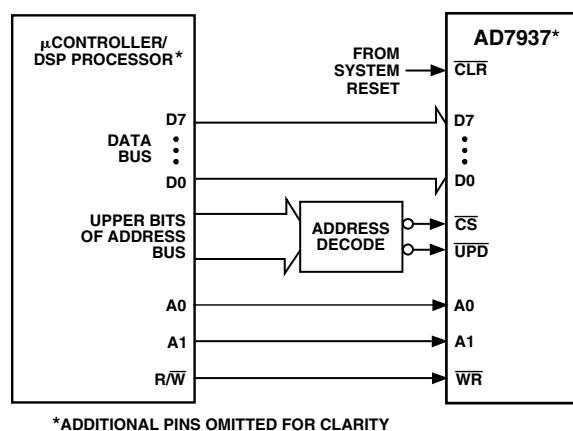

*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 8. AD7937 8-Bit Interface

AD7937

Dimensions shown in inches and (mm).

24-Lead Small Outline SOIC
(R-24)

0.6141 (15.60)
0.5985 (15.20)

24   13

0.2992 (7.60)
0.2914 (7.40)

0.4193 (10.65)
0.3937 (10.00)

1   12

PIN 1

0.1043 (2.65)
0.0926 (2.35)

0.0291 (0.74)
0.0098 (0.25) × 45°

0.0118 (0.30)
0.0040 (0.10)

0.0500
(1.27)
BSC

0.0192 (0.49)
0.0138 (0.35)

SEATING
PLANE

0.0125 (0.32)
0.0091 (0.23)

8°
0°

0.0500 (1.27)
0.0157 (0.40)

REV. 0