

N-channel 55 V, 0.0065 Ω typ., 78 A STripFET™ II
Power MOSFETs in D²PAK and TO-220 packages

Datasheet — production data

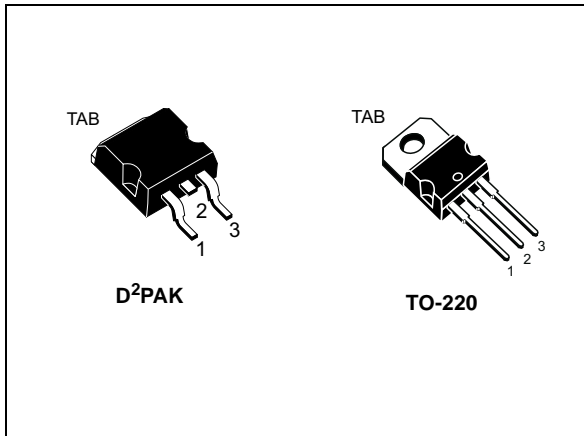
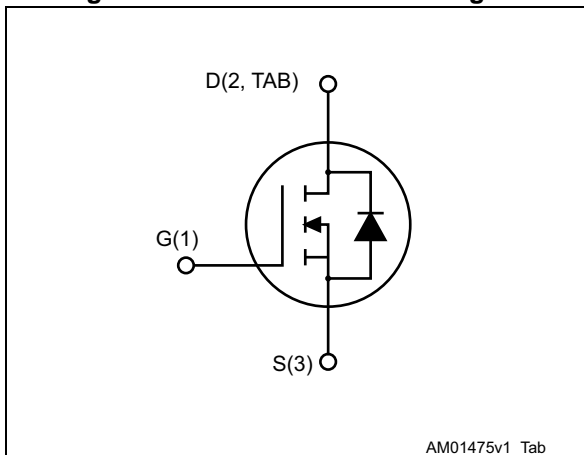


Figure 1. Internal schematic diagram



Features

Order code	V _{DSS}	R _{DS(on)} max	I _D
STB78NF55-08	55 V	0.008 Ω	80 A
STP78NF55-08			

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

These Power MOSFETs have been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the devices suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Table 1. Device summary

Order code	Marking	Packages	Packing
STB78NF55-08	78NF55-08	D ² PAK	Tape and reel
STP78NF55-08	78NF55-08	TO-220	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	55	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	80	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	80	A
$I_{DM}^{(2)}$	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	300	W
T_{stg}	Operating junction temperature range	- 55 to 175	$^\circ\text{C}$
T_j	Storage temperature range		

1. Current limited package
2. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		D ² PAK	TO-220	
$R_{thj-case}$	Thermal resistance junction-case	0.5		$^\circ\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb	35 ⁽¹⁾		$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient		62.5	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch² FR-4 board, 2 oz Cu

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	40	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25\text{ }^\circ\text{C}$, $I_D=I_{AS}$, $V_{DD}=30\text{ V}$)	1000	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	55			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 55\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 55\text{ V}$, @ 125 °C (1)			10	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$ $V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 40\text{ A}$		0.0065	0.008	Ω

1. Defined by design, not subject to production test

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}$, $I_D = 18\text{ A}$	-	40	-	S
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$		3740		pF
C_{oss}	Output capacitance		-	830	-	pF
C_{riss}	Reverse transfer capacitance		-	265	-	pF
Q_g	Total gate charge	$V_{DD} = 27\text{ V}$, $I_D = 80\text{ A}$,	-	112	155	nC
Q_{gs}	Gate-source charge	$V_{GS} = 10\text{ V}$,	-	20	-	nC
Q_{gd}	Gate-drain charge	(<i>Figure 14: Gate charge test circuit</i>)	-	40	-	nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 7. Switching times

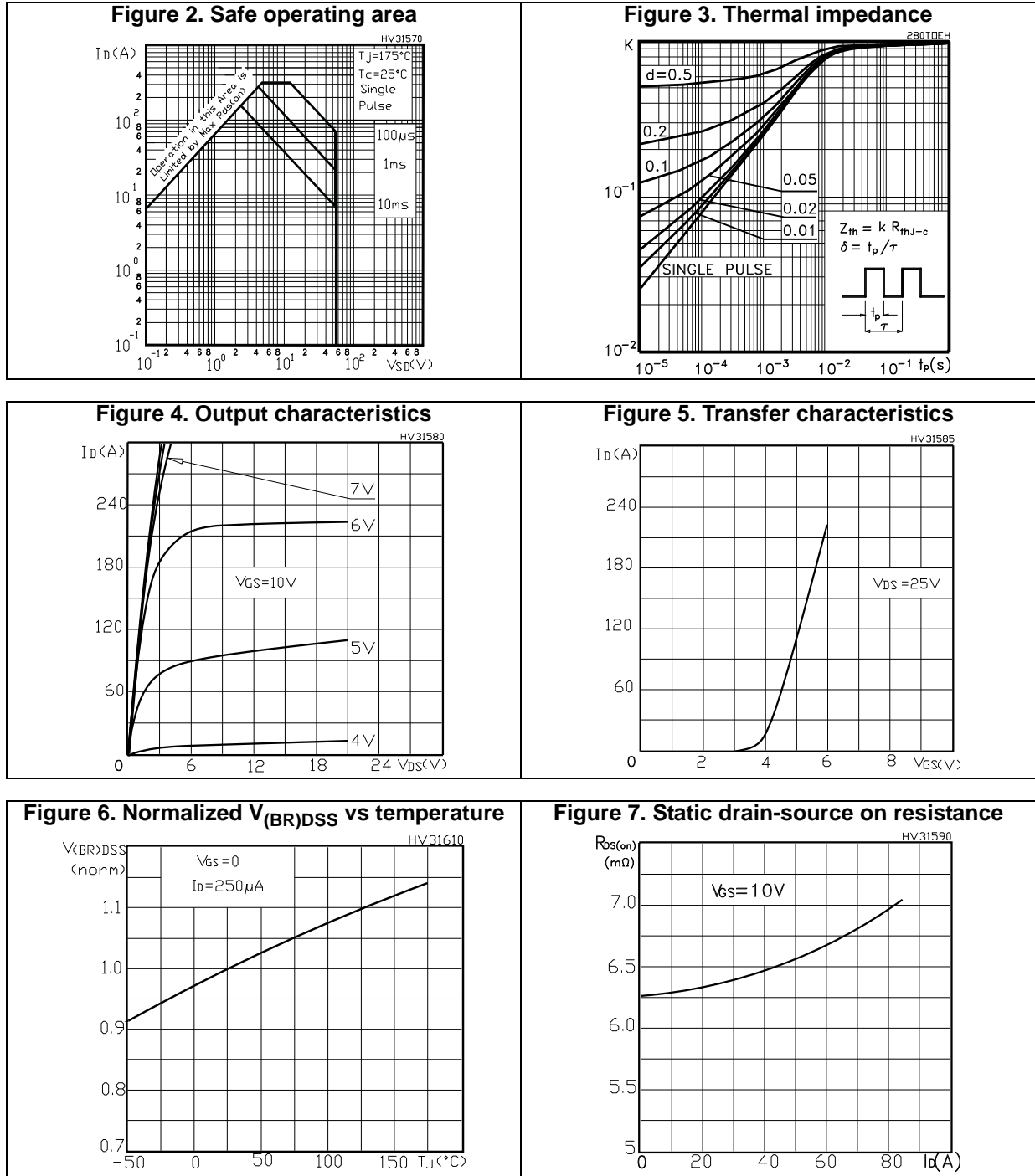
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 27\text{ V}$, $I_D = 40\text{ A}$ $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (<i>Figure 13: Switching times test circuit for resistive load and Figure 18: Switching time waveform.</i>)	-	20	-	ns
t_r	Rise time		-	110	-	ns
$t_{d(off)}$	Turn-off delay time		-	75	-	ns
t_f	Fall time		-	35	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		80	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		320	A
V_{SD}	Forward on voltage	$I_{SD} = 80 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.5	V
$t_{rr}^{(2)}$	Reverse recovery time	$I_{SD} = 80 \text{ A}$, $V_{DD} = 25 \text{ V}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $T_j = 150 \text{ }^\circ\text{C}$ (<i>Figure 15: Test circuit for inductive load switching and diode recovery times</i>)	-	80		ns
Q_{rr}	Reverse recovery charge		-	230		nC
I_{RRM}	Reverse recovery current		-	5.7		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)



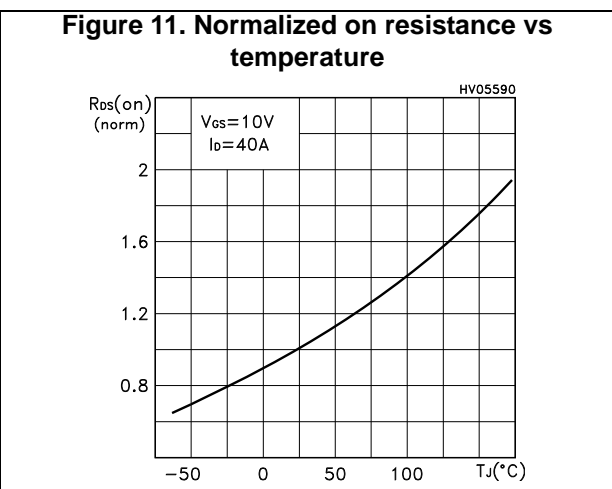
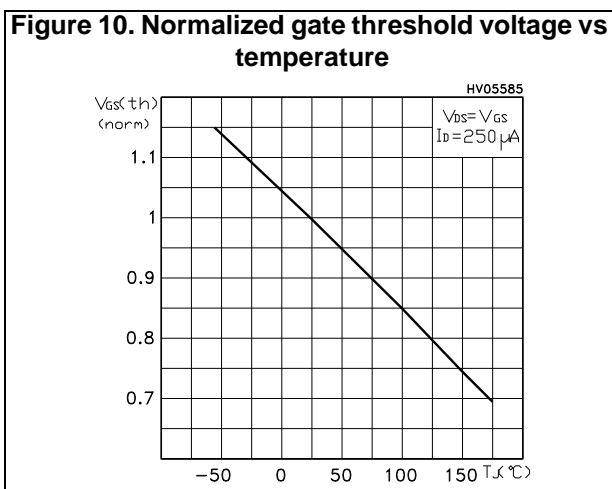
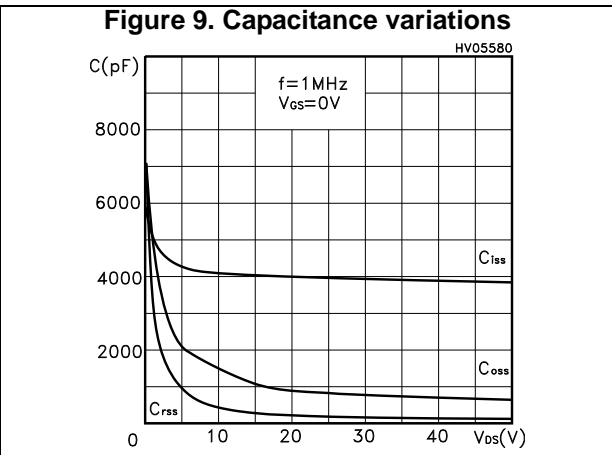
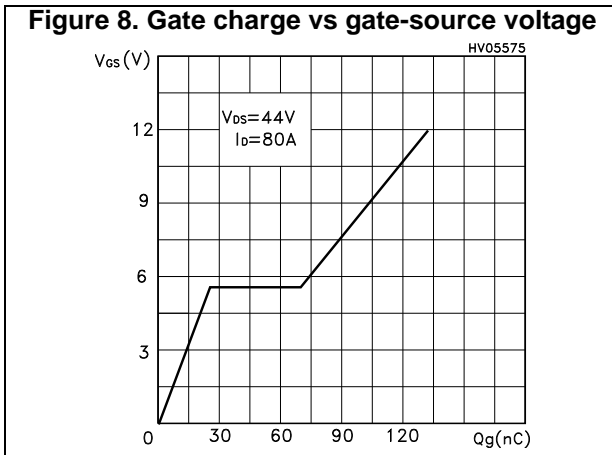
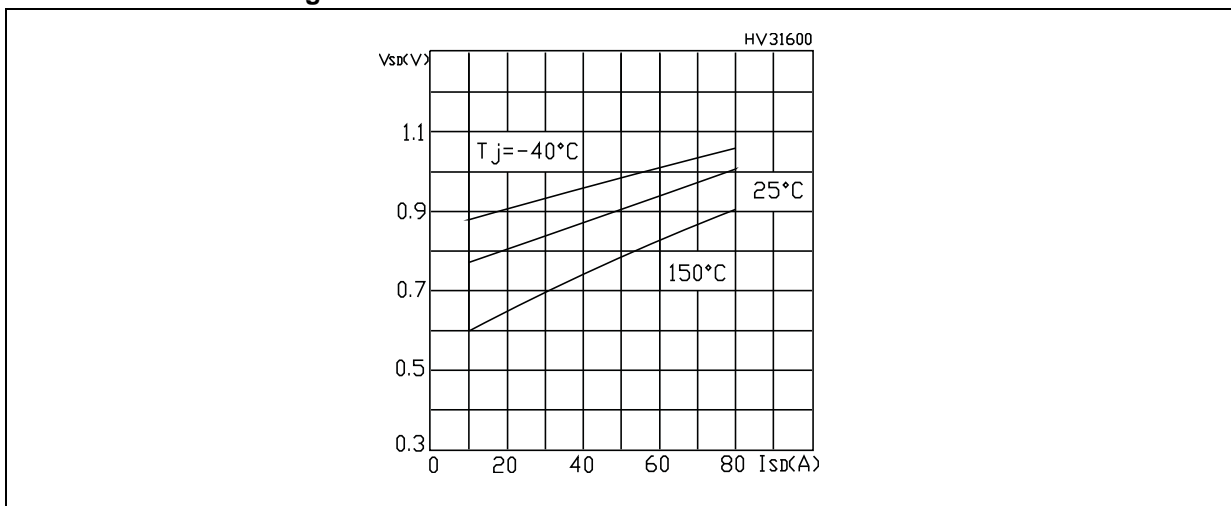
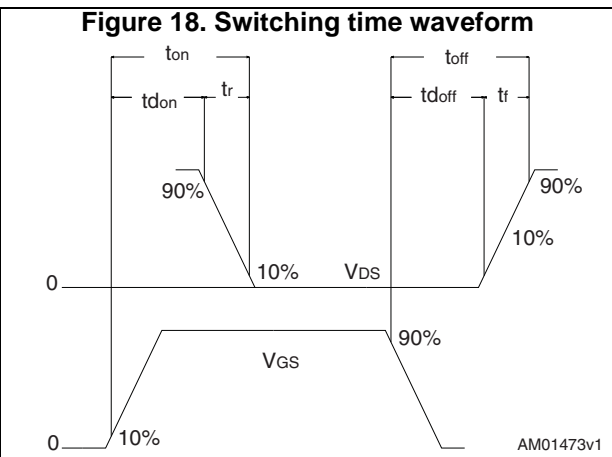
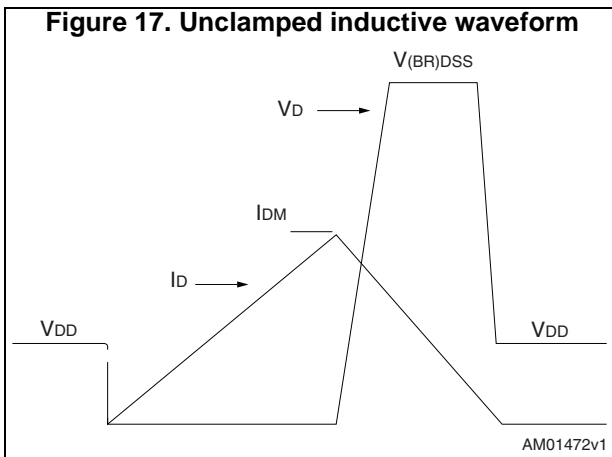
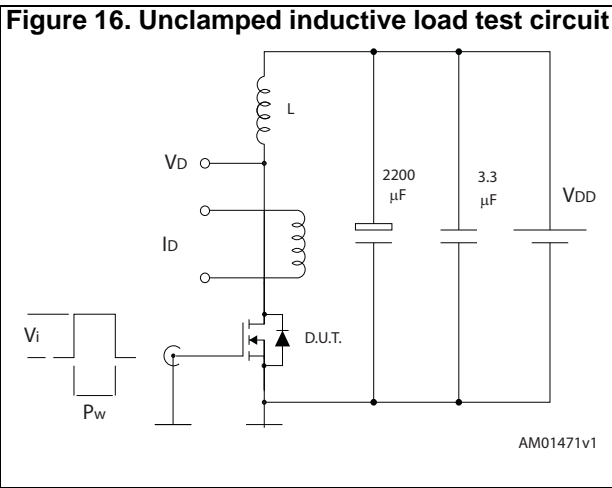
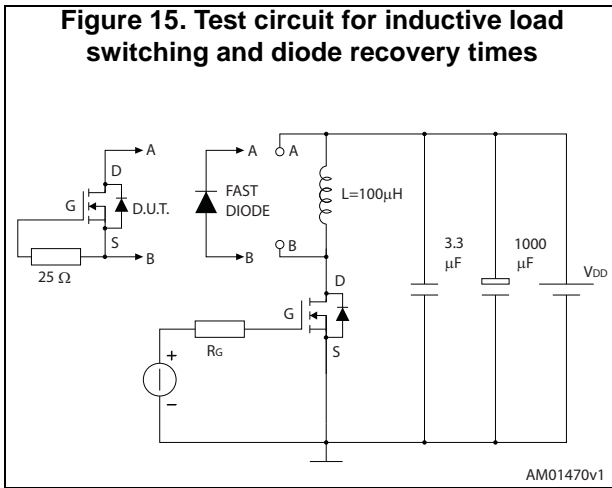
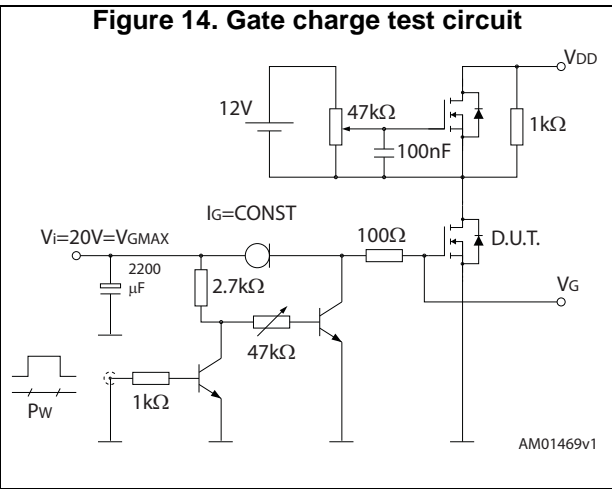
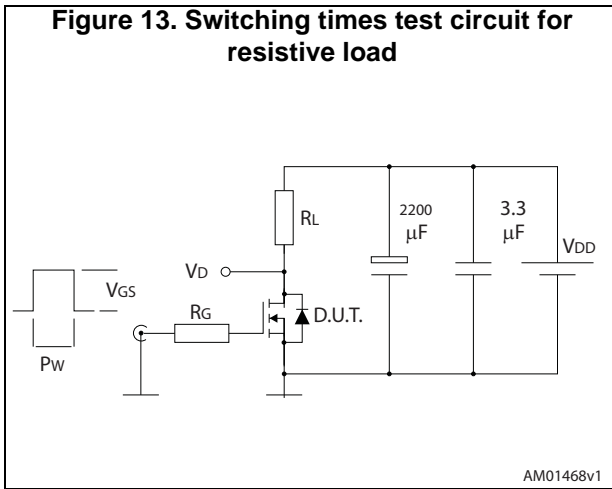


Figure 12. Source-drain diode forward characteristics



3 Test circuits



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 D²PAK package information

Figure 19. D²PAK (TO-263) type A package outline

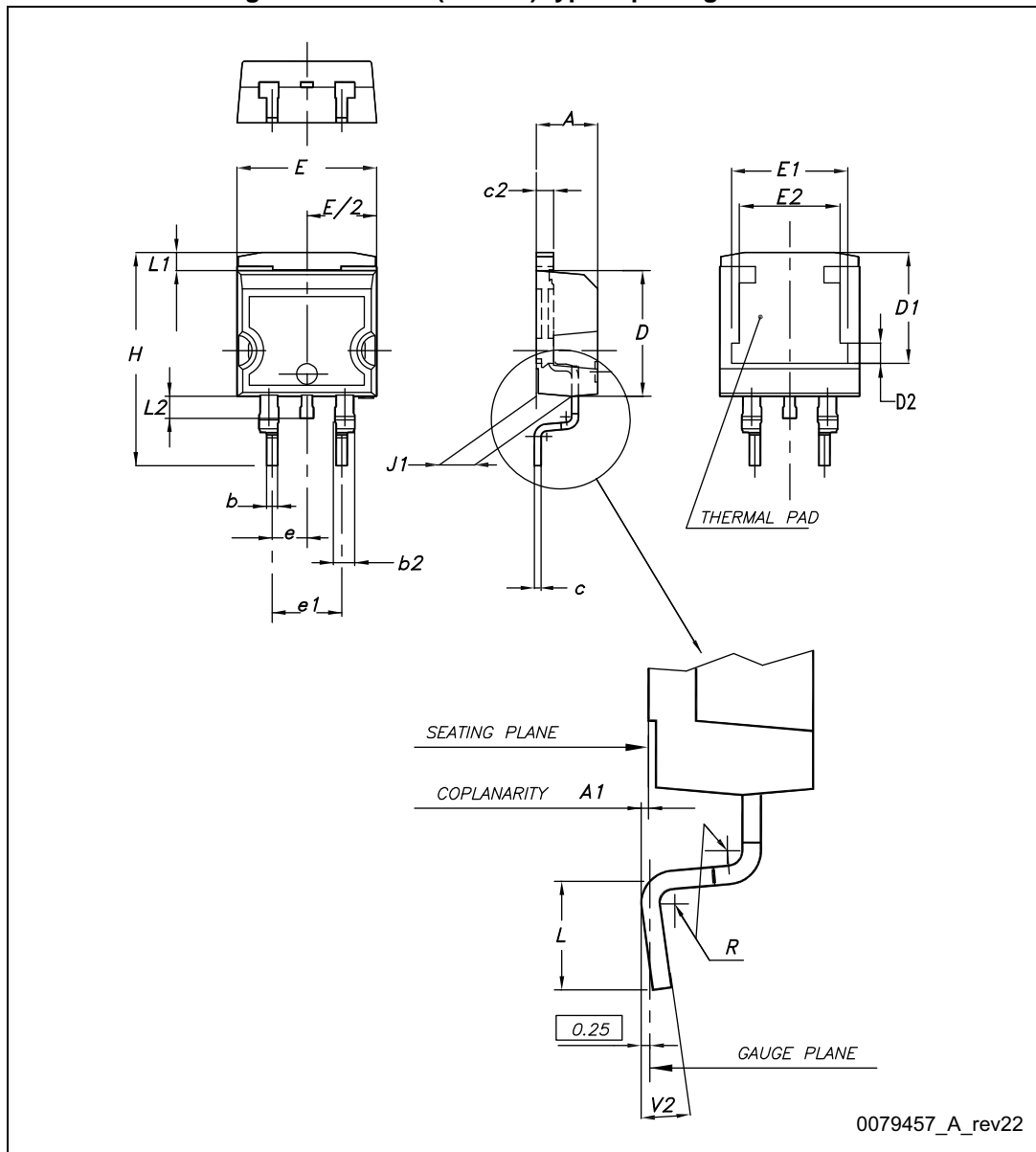
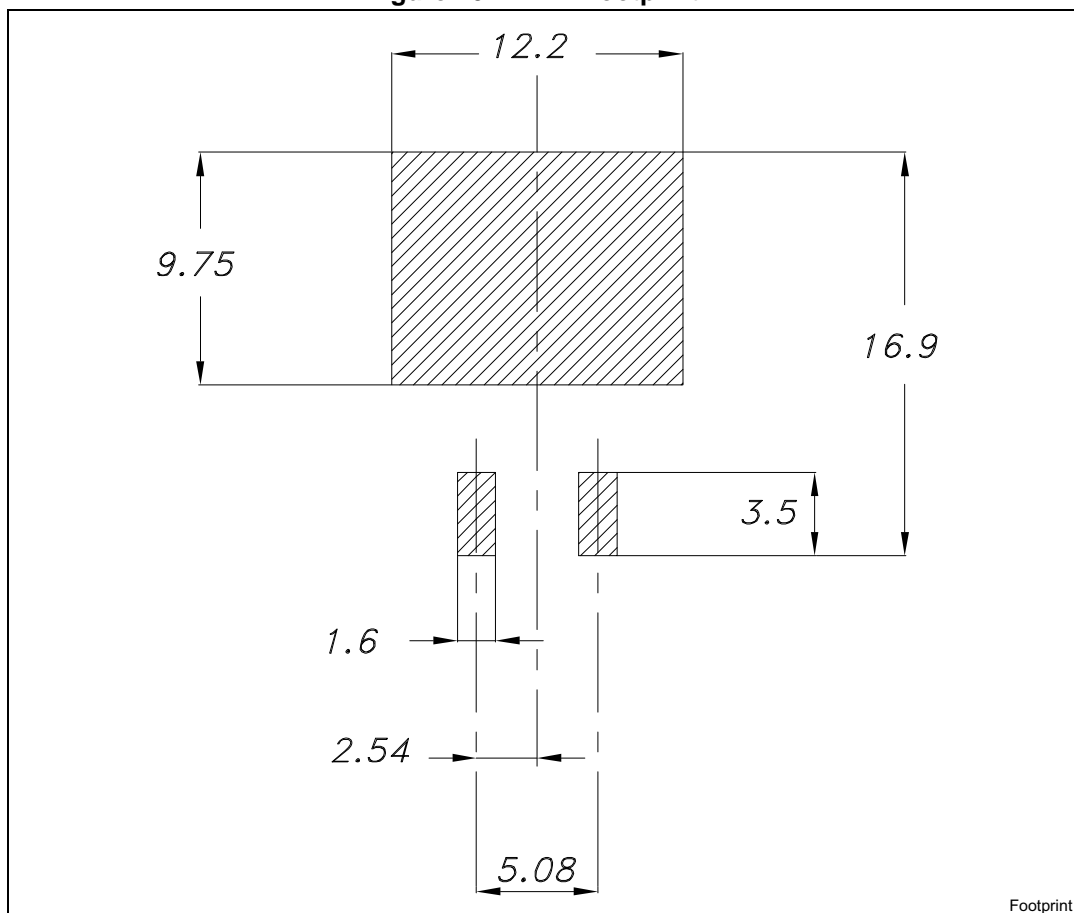


Table 9. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

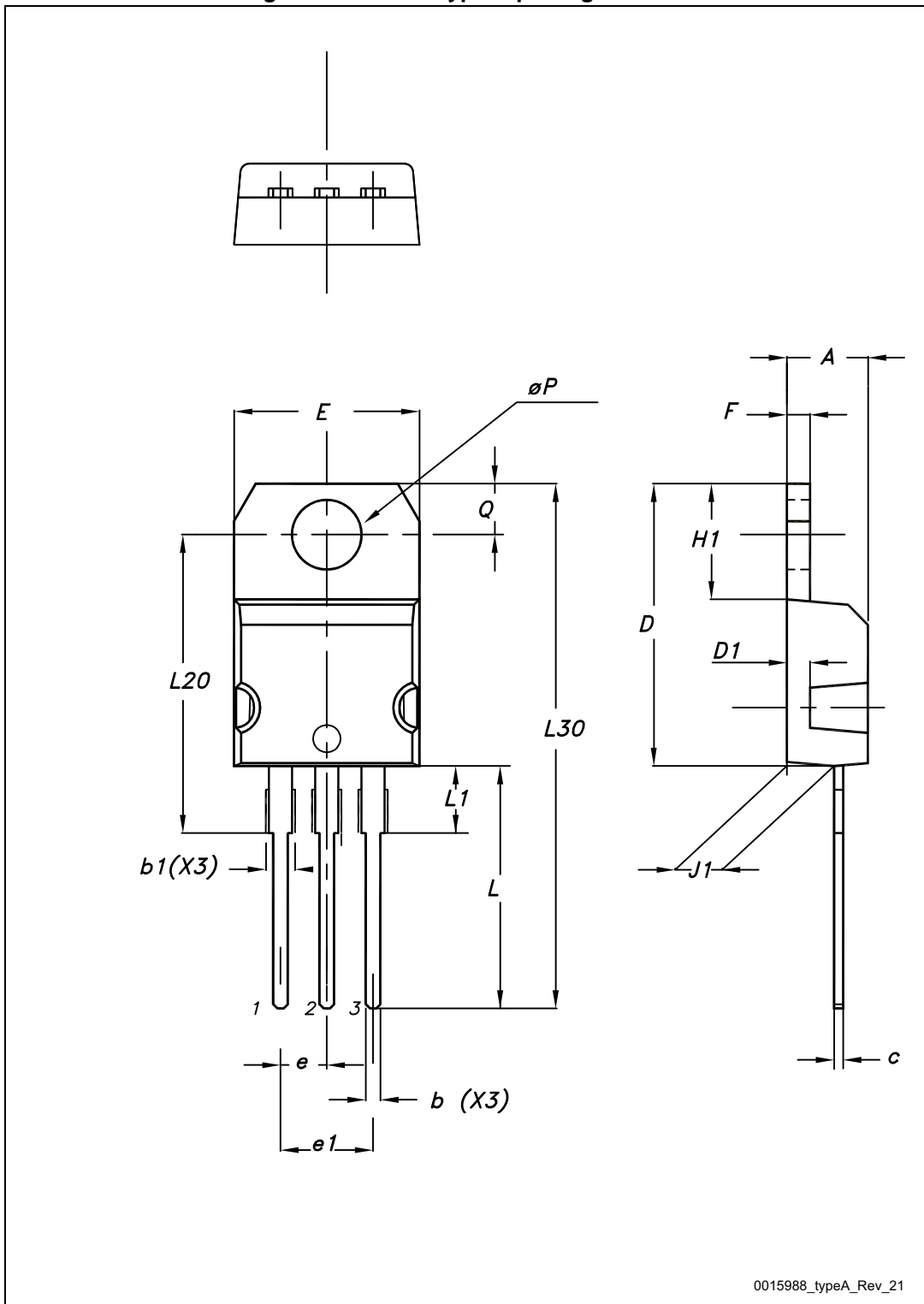
Figure 20. D²PAK footprint^(a)



a. All dimension are in millimeters

4.2 TO-220 type A package information

Figure 21. TO-220 type A package outline



0015988_typeA_Rev_21

Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.3 TO-220 type B package information

Figure 22. TO-220 type B package outline

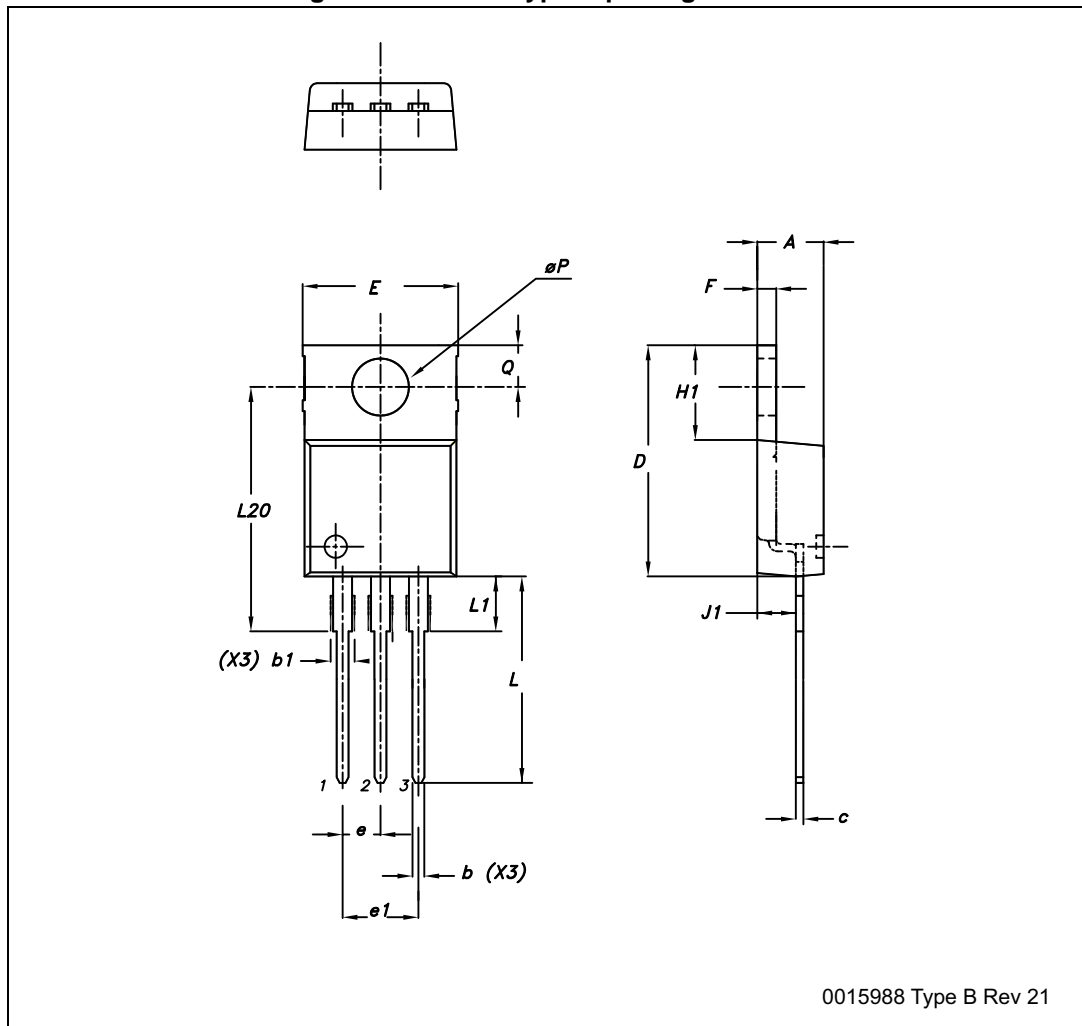


Table 11. TO-220 type B package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.60
b	0.70		0.89
b1	1.19		1.35
c	0.31		0.46
D	14.80		15.10
E	10.20		10.37
e		2.54	
e1	5.00		5.14
F	1.21		1.32
H1	6.20		6.40
J1		2.66	
L	13.70		14.00
L1	3.40		3.94
L20		15.87	
øP	3.78		3.89
Q	2.69		2.80

5 Packing information

Figure 23. Tape

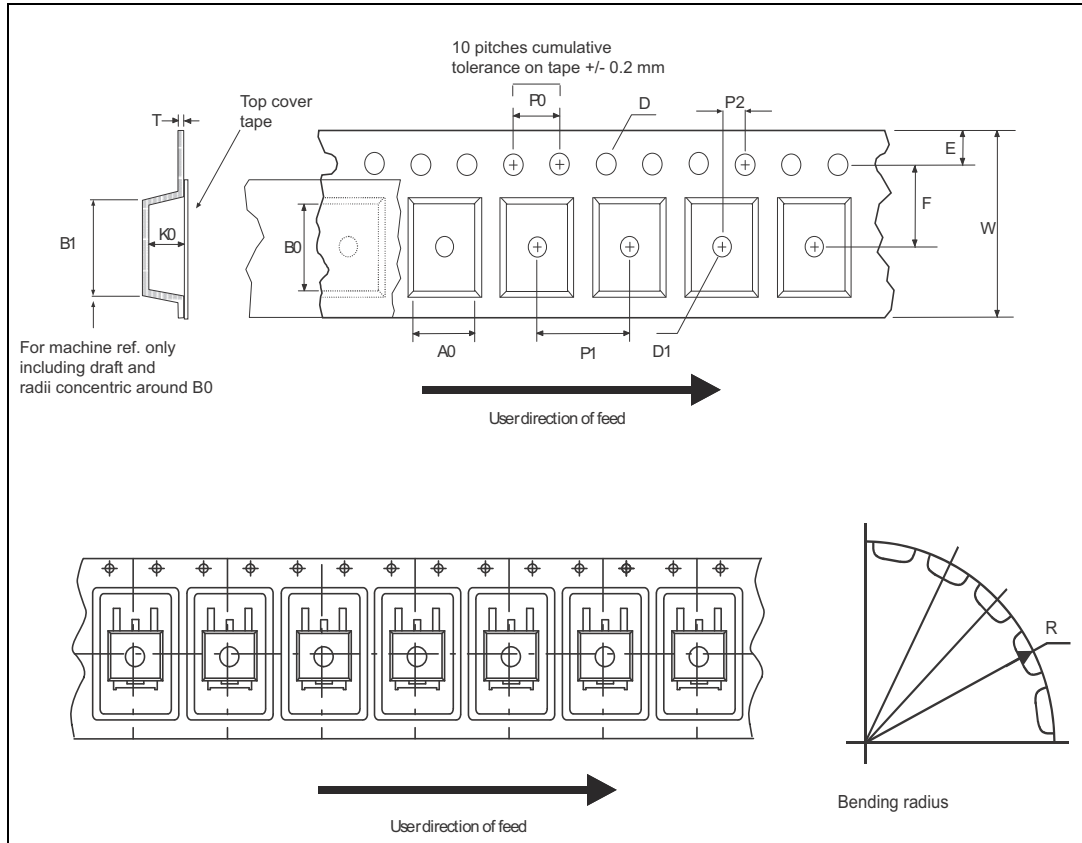
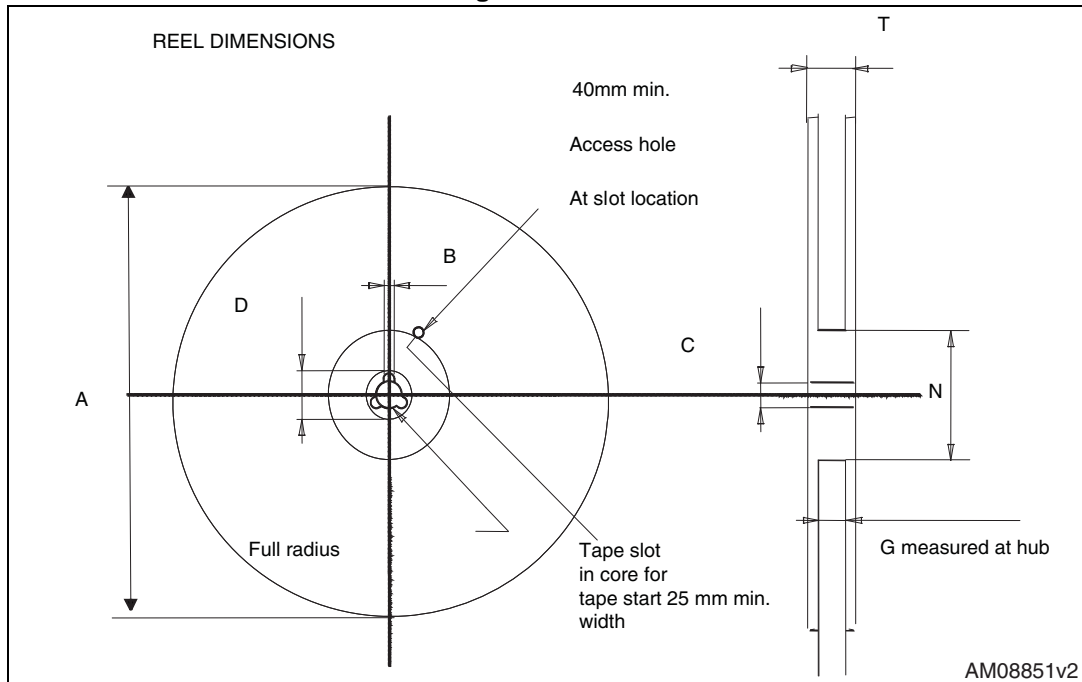


Figure 24. Reel



AM08851v2

Table 12. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

6 Revision history

Figure 25. Document revision history

Date	Revision	Changes
19-Jul-2016	1	First release

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