FEDL9090A-01

LAPIS Semiconductor

This version: May 2001

ML9090A-01, -02

LCD Driver with Key Scanner and RAM

GENERAL DESCRIPTION

The ML9090A-01 and ML9090A-02 are LCD drivers that contain internal RAM and a key scan function. They are best suited for car audio displays.
Since 1-bit data of the display data RAM corresponds to the light-on or light-off of 1-dot of the LCD panel (a bit map system), a flexible display is possible.
A single chip can implement a graphic display system of a maximum of 80 × 18 dots (80 × 10 dots for the ML9090A-01, 80 × 18 dots for the ML9090A-02).
Since containing voltage multipliers, the ML9090A-01 and ML9090A-02 require no power supply circuit to drive the LCD.
Since the internal 5 × 5 scan circuit has eliminated the needs of key scanning by the CPU, the ports of the CPU can be efficiently used.

FEATURES

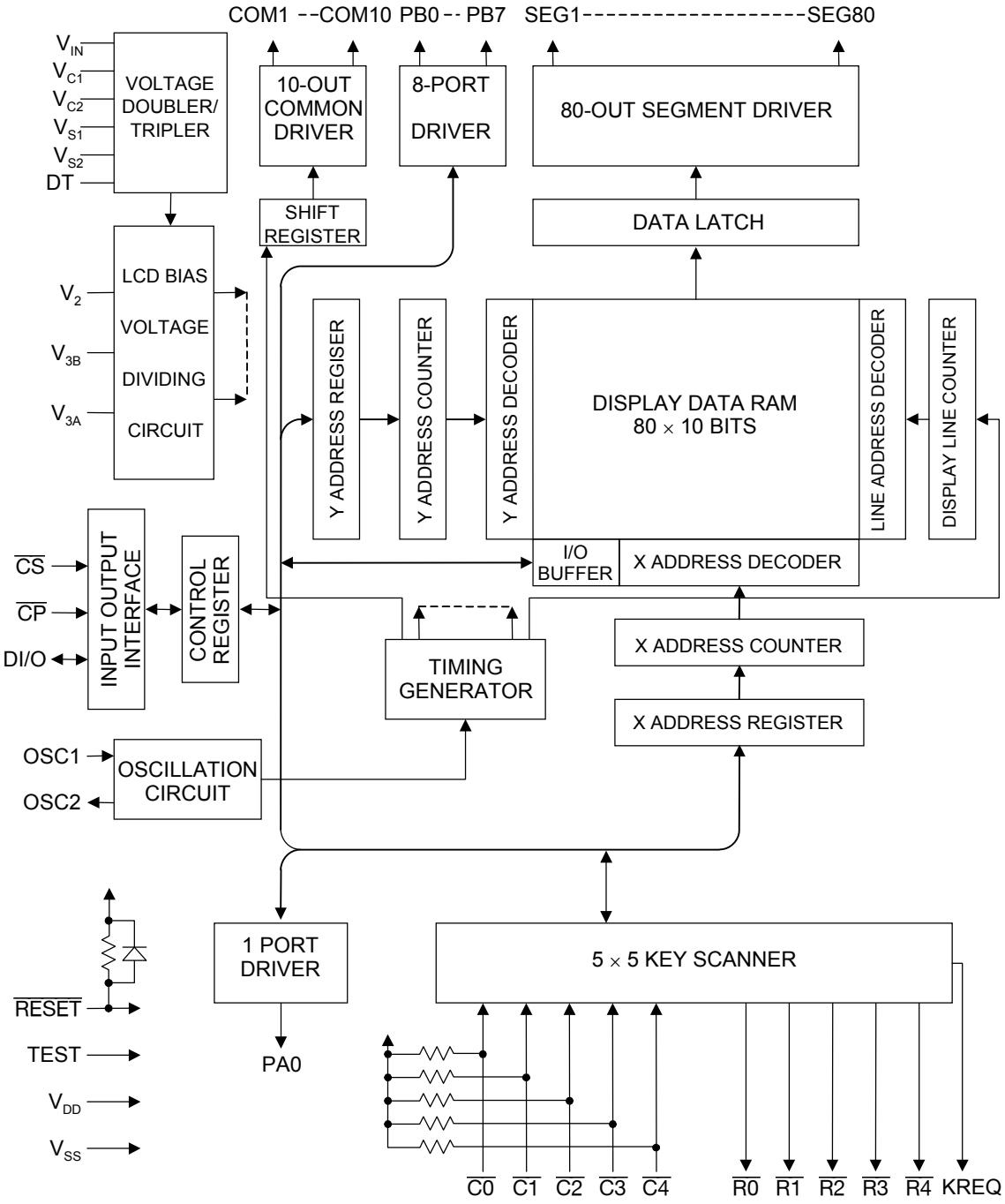
- Logic voltage: 2.7 to 5.5 V
- LCD drive voltage: 6 to 16 V (positive voltage)
- 80 segment outputs, 10 common outputs for ML9090A-01 and 18 common outputs for ML9090A-02
- Built-in bit-mapped RAM (ML9090A-01: 80 × 10 = 800 bits, ML9090A-02: 80 × 18 = 1440 bits)
- 4-pin serial interface with CPU: $\overline{CS}$, $\overline{CP}$, DI/O, KREQ
- Built-in LCD drive bias resistors
- Built-in voltage doubler or tripler circuit
- Built-in 5 × 5 key scanner
- Port A output : 1 pin, output current: –15 mA: (may be used for LED driving)
- Port B output : 8 pins
  Output current (available for the ML9090A-01 only)
  –2 mA : 5 pins
  –15 mA : 3 pins
- Temperature range: –40 to +85°C
- Package: 128-pin plastic QFP (QFP128-P-1420-0.50-K) (Product name: ML9090A-01GA)
  (Product name: ML9090A-02GA)

Comparison between the ML9090A-01 and the ML9090A-02

Item	ML9090A-01	ML9090A-02
Number of common outputs	10 Max.	18 Max.
Number of dots on the LCD screen (selectable by program)	8 × 80 9 × 80 10 × 80	16 × 80 17 × 80 18 × 80
Number of port A outputs	1	1
Number of port B outputs	8	—

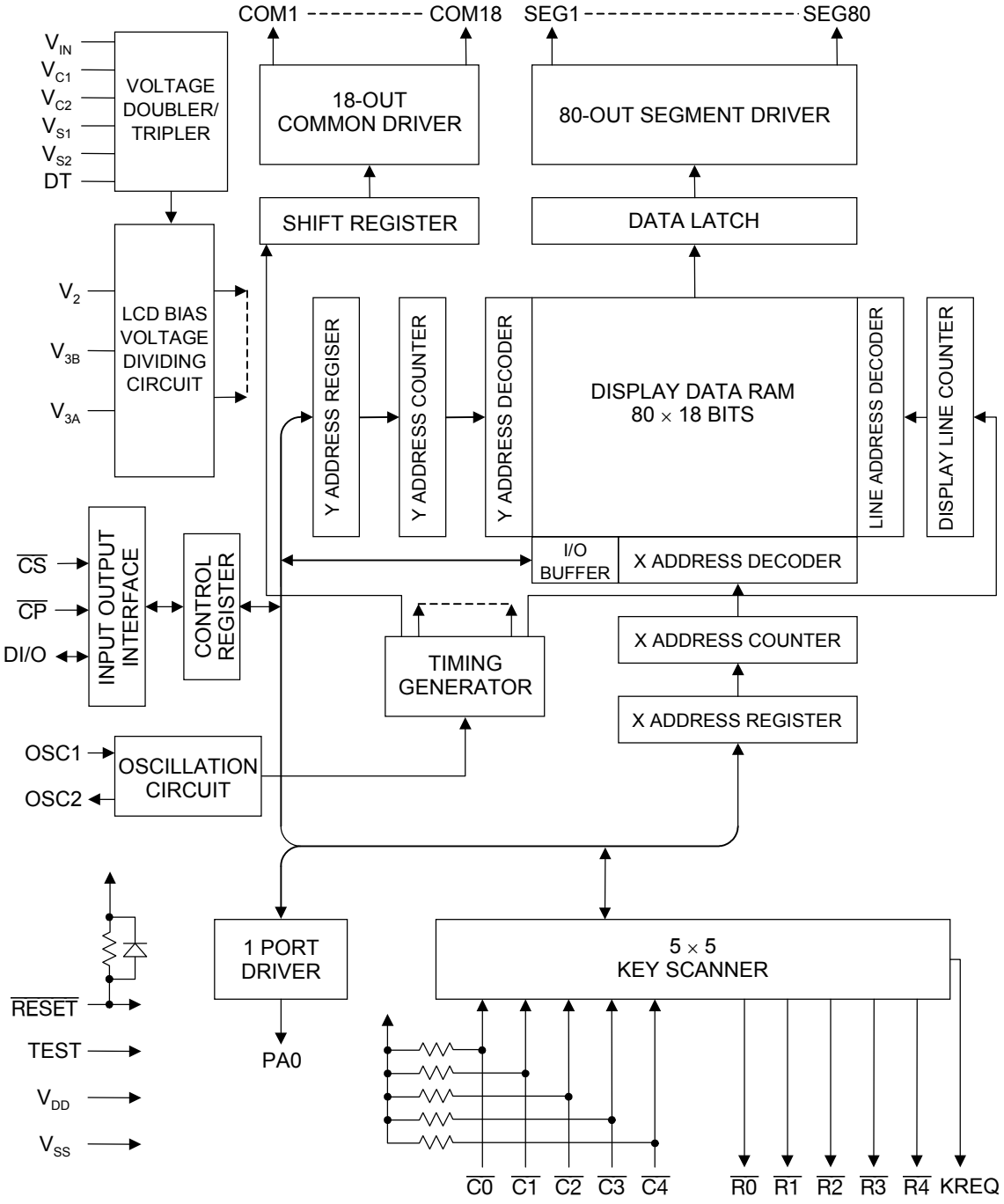
BLOCK DIAGRAM (1/2)

ML9090A-01



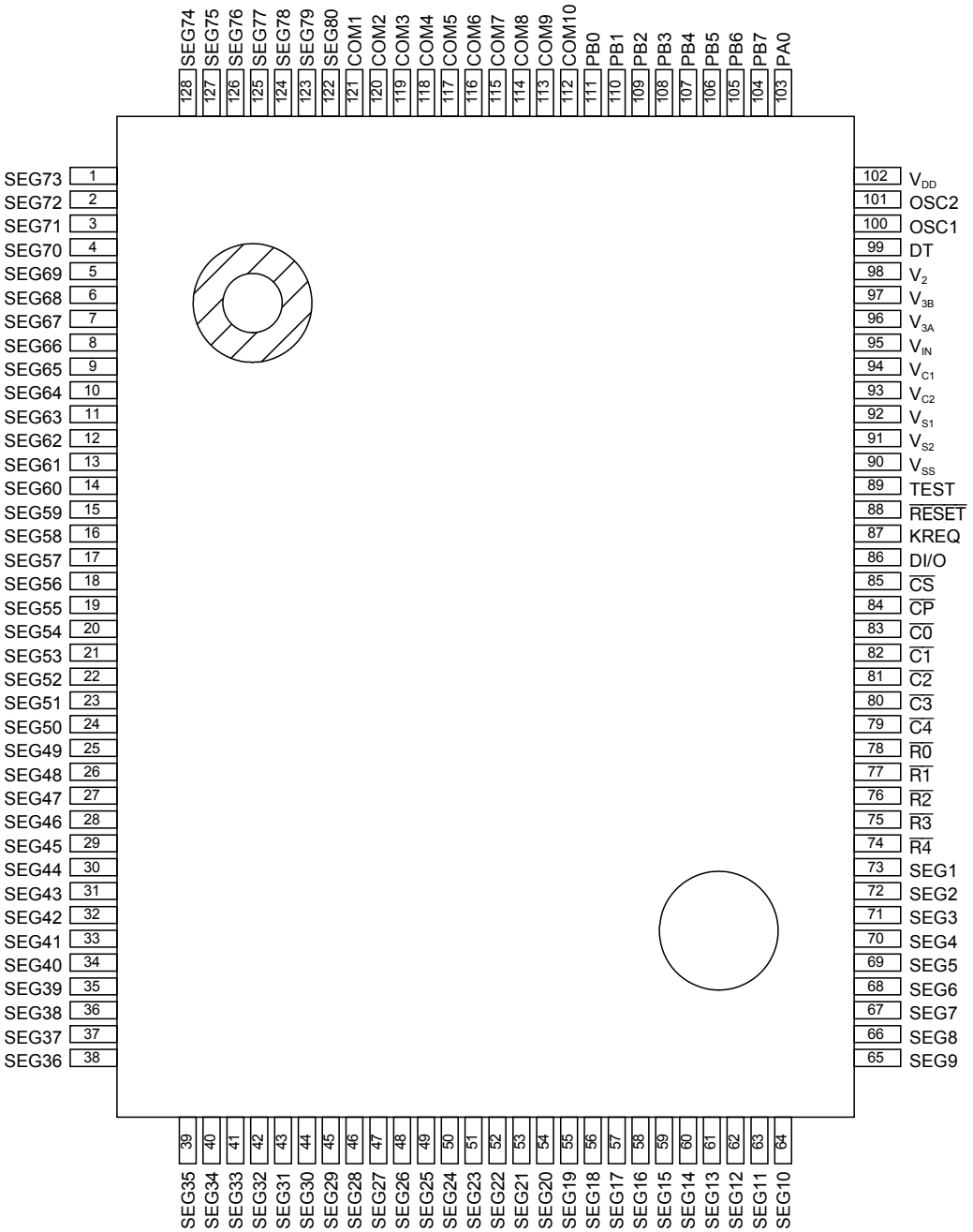
BLOCK DIAGRAM (2/2)

ML9090A-02



PIN CONFIGURATION (TOP VIEW) 1/2

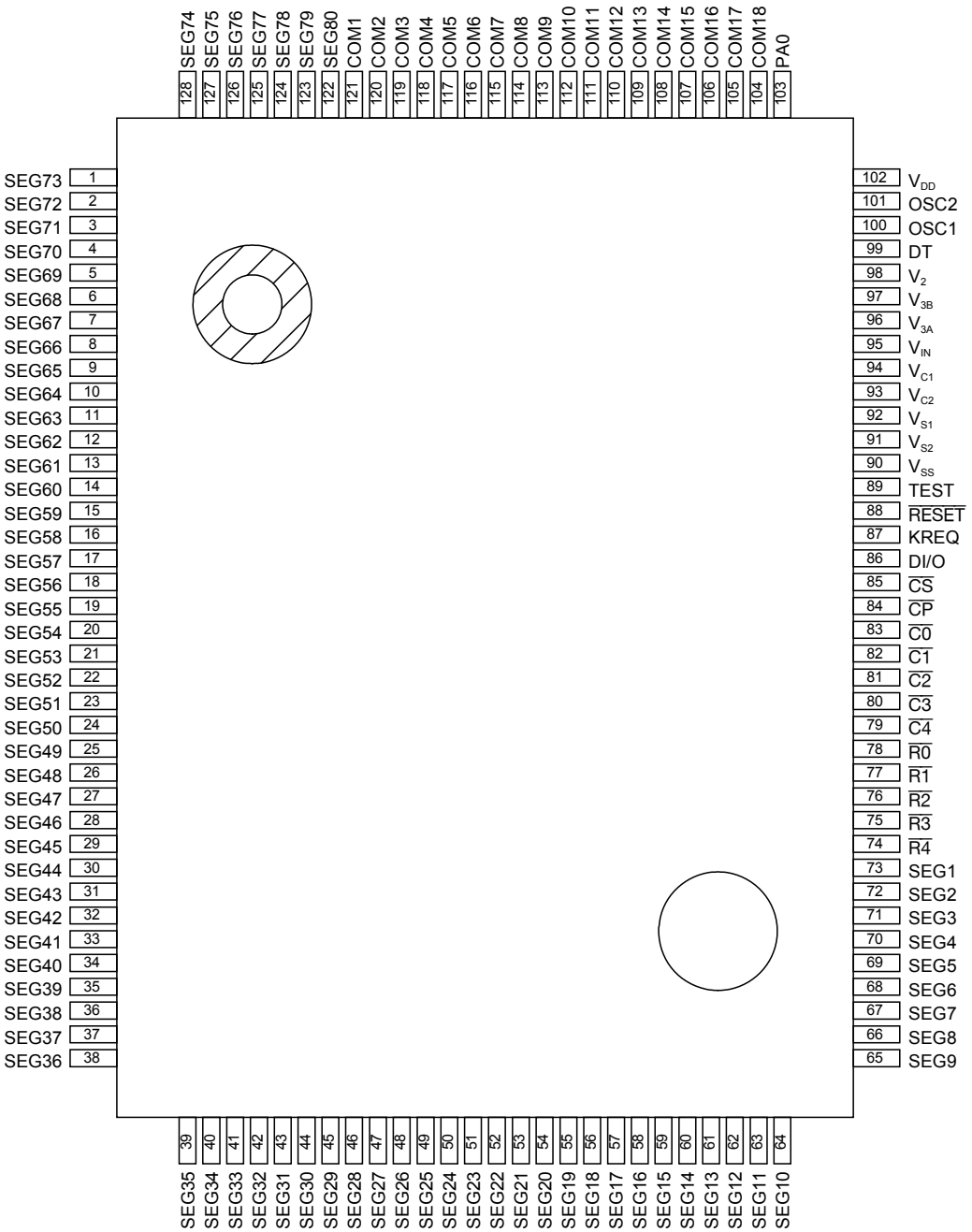
ML9090A-01



128-pin plastic QFP

PIN CONFIGURATION (TOP VIEW) 2/2

ML9090A-02



128-pin plastic QFP

FUNCTIONAL DESCRIPTIONS

Pin Functional Descriptions

Function	Pin	Symbol	Type	Description
CPU interface	85	$\overline{CS}$	I	Chip select signal input pin
	84	$\overline{CP}$	I	Shift clock signal input pin. This pin is connected to an internal Schmitt circuit
	86	DI/O	I/O	Serial data signal I/O pin
	87	KREQ	O	Key request signal output pin
Oscillation	100	OSC1	I	Connect external resistors. If using an external clock, input it from the OSC1 pin and leave the OSC2 pin open.
	101	OSC2	O	
Control signals	88	$\overline{RESET}$	I	Initial settings can be established by pulling the reset input to a “L” level. This pin is connected to an internal Schmitt circuit.
	99	DT	I	Input pin for selecting the voltage doubler or voltage tripler.
	89	TEST	I	Test input pin. This pin is connected to the V_{SS} pin.
Key scan signals	83 to 79	$\overline{C0}$ to $\overline{C4}$	I	Input pins that detect status of key switches
	78 to 74	$\overline{R0}$ to $\overline{R4}$	O	Key switch scan signal output pins
Port outputs	103	PA0	O	Port A output
	111 to 104	PB0 to PB7	O	Port B outputs (for ML9090A-01)
LCD driver outputs	73 to 122	SEG1 to SEG80	O	Outputs for LCD segment drivers
	121 to 112	COM1 to COM10	O	Outputs for LCD common drivers (for ML9090A-01)
	121 to 104	COM1 to COM18	O	Outputs for LCD common drivers (for ML9090A-02)
Power supply	102	V_{DD}	—	Logic power supply pin
	90	V_{SS}	—	GND pin
	95	V_{IN}	—	Voltage multiplier reference voltage power supply pin
	94, 93	V_{C1}, V_{C2}	—	Capacitor connection pins for voltage multiplier
	92	V_{S1}	—	Voltage multiplier output pin
	91	V_{S2}	—	Voltage multiplier output pin
	98, 96, 97	V_2, V_{3A}, V_{3B}	—	LCD bias pins

Pin Functional Descriptions

- **$\overline{CS}$**

Chip select input pin. An "L" level selects the chip, and an "H" level does not select the chip. During the "L" level, internal registers can be accessed.

- **$\overline{CP}$**

Clock input pin for serial interface data I/O. An internal Schmitt circuit is connected to this pin. Data input to the DI/O pin is synchronized to the rising edge of the clock. Output from the DI/O pin is synchronized to the falling edge of the clock.

- **DI/O**

Serial interface data I/O pin. This pin is in the output state only during the interval beginning when key scan data read or RAM read commands are written until the $\overline{CS}$ signal rises. At all other times this pin is in the input state. (When reset, the input state is set.) In other words, this pin goes into the output state only when the key scan register or the display data RAM is read. The relation between data level of this pin and operation is listed below.

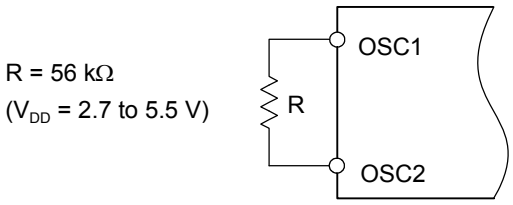
Data level	LCD display	Port	Key status
"H"	Light ON	"H"	ON
"L"	Light OFF	"L"	OFF

- **KREQ**

Key scan read READY signal output pin. Two scan cycles after a key switch is switched ON, this pin goes to an "H" level. When all key switches are OFF, this pin returns to an "L" level.
This signal can be used as a flag. To use it as a flag, start the key-scan reading when the KREQ signal changes to an "H" level from an "L" level. If the key-scan reading starts when the KREQ signal changes to an "L" level from an "H" level, scanned data may be unstable. To avoid this, repeat the key-scan reading three times.
When the key-scan reading starts when this pin goes to an "L" level, data when a key switch is off is read.

- **OSC1**

Input pin for RC oscillation. An oscillation circuit is formed by connecting a resistor (R) of 56kΩ ±2% to this pin and the OSC2 pin. If an external master oscillation clock is to be input, input the master oscillation clock to this pin.



- **OSC2**

Output pin for RC oscillation. An oscillation circuit is formed by connecting a resistor (R) of 56kΩ ±2% to this pin and the OSC1 pin. If an external master oscillation clock is to be input, leave this pin unconnected (open).

- **$\overline{\text{RESE}}$**

Reset signal input pin. The initial state can be set by pulling this pin to an "L" level. Refer to the "Output, I/O and Register States in Response to Reset Input" page for the initial states of each register and display.
An internal pull-up resistor is connected to this pin. An external capacitor is connected for power-on-reset operation.

- **TEST**

Test signal input pin. This pin is used for testing by LAPIS Semiconductor. Connect this pin to V_{SS}. When a different connection is made, proper operation cannot be guaranteed.

- **$\overline{\text{R0}}$ to $\overline{\text{R4}}$**

Key switch scan signal output pins. During the scan operation, "L" level signals are output in the order of R0, R1, ...R4. (Refer to the page entitled "Key scan" for details.)

- **$\overline{\text{C0}}$ to $\overline{\text{C4}}$**

Input pins that detect the key switch status. Internal pull-up resistors are connected to these pins. Assemble a key matrix between these pins and the $\overline{\text{R0}}$ to $\overline{\text{R4}}$ pins.

- **PA0**

General-purpose port A output pin. Because this pin can output a current of –15 mA, it is best suited as an LED driver. If this pin is used as an LED driver, insert an external current limiting resistor in series with the LED. If this pin is not used, leave it unconnected (open).

- **PB0 to PB7**

General-purpose port B output pins. Each of the PB5 to PB7 pins has the same driving capability as the PA0 pin, namely the ability to output a current of –15 mA. These pins are only applicable to the ML9090A-01. Leave unused pins unconnected (open).

- **SEG1 to SEG80**

Segment signal output pins for LCD driving. Leave unused pins unconnected (open).

- **COM1 to COM18**

Common signal output pins for LCD driving. Leave unused pins unconnected (open). COM11 to COM18 are provided for the ML9090A-02 and PB0 to PB7 for the ML9090A-01.

- **V_{DD}**

Logic power supply connection pin.

- **V_{SS}**

Power supply GND connection pin.

- **DT**

This pin selects the voltage multiplier circuit. If this pin is connected to the V_{SS} pin, the voltage doubler circuit is selected. If this pin is connected to the V_{DD} pin, the voltage tripler circuit is selected. Do not change the value of the setting after power is turned on.

- **V_{C1}, V_{C2}**

Capacitor connection pins for the voltage multiplier. Connect a 4.7 μF capacitor between the V_{C1} and V_{C2} pins. If an electrolytic capacitor is used, connect the (+) side to pin V_{C2}.

- **V_{S1}**

Voltage doubler voltage output pin. This pin outputs the doubled voltage that has been input to V_{IN}. To increase stability of the power supply, connect a 4.7 μF capacitor between this pin and V_{SS}. When using the doubled voltage, connect this pin and V_{S2}.

- **V_{S2}**

Voltage multiplier voltage output pin. Voltage multiplied by the factor specified by the DT pin setting is output from this pin. When the voltage tripler is used, to increase stability of the power supply, connect a 4.7 μF capacitor between this pin and V_{SS}. When using the voltage doubler, connect this pin and V_{S1}.

- **V_{IN}**

Voltage multiplier voltage input pin. The doubled or tripled voltage input to this pin is output from V_{S1} or V_{S2}.

- **V_2, V_{3A}, V_{3B}**

LCD bias pins for segment drivers. These pins are connected to internal bias dividing resistors. When using the ML9090A-01 (at 1/4 bias), connect V_2 and V_{3A} pins, and leave V_{3B} unconnected (open). When using the ML9090A-02 (at 1/5 bias), connect V_{3A} and V_{3B} pins, and leave V_2 unconnected (open).

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit	Applicable Pins
Power Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to +7.0	V	V_{DD}
Bias Voltage	V_{BI}	Ta = 25°C	–0.3 to +18.0	V	V_{C1}, V_{C2}, V_{S1}, V_{S2}, V_2,V_{3A}, V_{3B}
Voltage Multiplier ReferenceVoltage	V_{IN}	Ta = 25°C *1	–0.3 to +9.0	V	V_{IN}
		Ta = 25°C *2	–0.3 to +6.0		
Input Voltage	V_I	Ta = 25°C	–0.3 to V_{DD} +0.3	V	$\overline{CS}$, $\overline{CP}$, DI/O,OSC1, $\overline{RESET}$, DT,TEST, $\overline{C0}$ to $\overline{C4}$
Output Current	I_O	Ta = 25°C	–20	mA	PA0, PB5 to PB7
		Ta = 25°C	–3	mA	PB0 to PB4
Power Dissipation	P_D	Ta = 85°C	190	mW	—
Storage Temperature	T_{stg}	—	–55 to +150	°C	—

V_{SS} is the reference voltage potential for all pins.

*1: When the voltage doubler is used.
*2: When the voltage tripler is used.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit	Applicable Pins
Power Supply Voltage	V_{DD}	—	2.7 to 5.5	V	V_{DD}
Bias Voltage	V_{S2}	—	6.0 to 16.0	V	V_{S2}
Voltage Multiplier ReferenceVoltage	V_{IN}	*1	3.55 to 8.00	V	V_{IN}
		*2	2.84 to 5.33		
Operating Frequency	f_{op}	R = 56kΩ ±2%	480 to 1200	kHz	OSC1
Operating Temperature	T_{op}	—	–40 to +85	°C	—

V_{SS} is the reference voltage potential for all pins.

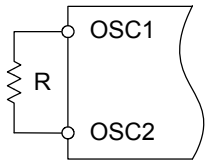
*1: When the voltage doubler is used.
*2: When the voltage tripler is used.

ELECTRICAL CHARACTERISTICS

OSC Circuit Operating Conditions

Parameter	Symbol	Condition	Rating	Unit	Applicable Pins
Oscillation Resistance	R	V_{DD} = 2.7 V to 5.5 V	56 *1	kΩ	OSC1, OSC2

*1: Use a resistor with an accuracy of ±2 %



ELECTRICAL CHARACTERISTICS

DC Characteristics

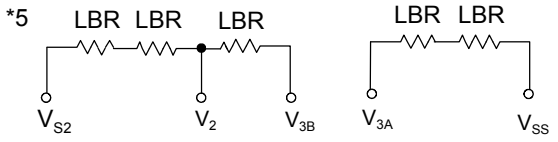
(V_{DD} = 2.7 to 5.5 V, V_{S2} = 6 to 16 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Pins
"H" Input Voltage 1	V_{IH1}	—	$0.85V_{DD}$	—	—	V	OSC1
"H" Input Voltage 2	V_{IH2}	—	$0.85V_{DD}$	—	—	V	$\overline{RESET}$
"H" Input Voltage 3	V_{IH3}	—	$0.85V_{DD}$	—	—	V	$\overline{CP}$
"H" Input Voltage 4	V_{IH4}	—	$0.8V_{DD}$	—	—	V	$\overline{CS}$, DI/O,$\overline{C0}$ to $\overline{C4}$
"L" Input Voltage 1	V_{IL1}	—	—	—	$0.15V_{DD}$	V	OSC1
"L" Input Voltage 2	V_{IL2}	—	—	—	$0.15V_{DD}$	V	$\overline{RESET}$
"L" Input Voltage 3	V_{IL3}	—	—	—	$0.15V_{DD}$	V	$\overline{CP}$
"L" Input Voltage 4	V_{IL4}	—	—	—	$0.2V_{DD}$	V	$\overline{CS}$, DI/O,$\overline{C0}$ to $\overline{C4}$
"H" Input Current 1	I_{IH1}	$V_I = V_{DD}$	—	—	10	μA	$\overline{RESET}$
"H" Input Current 2	I_{IH2}	$V_I = V_{DD}$	—	—	10	μA	$\overline{C0}$ to $\overline{C4}$
"H" Input Current 3	I_{IH3}	$V_I = V_{DD}$	—	—	10	μA	DI/O
"H" Input Current 4	I_{IH4}	$V_I = V_{DD}$	—	—	1	μA	OSC1, $\overline{CS}$, $\overline{CP}$,DT, TEST
"L" Input Current 1	I_{IL1}	V_{DD} = 5 V, V_I = 0 V	–0.02	–0.05	–0.1	mA	$\overline{RESET}$
"L" Input Current 2	I_{IL2}	V_{DD} = 5 V, V_I = 0 V	–0.18	–0.45	–0.9	mA	$\overline{C0}$ to $\overline{C4}$
"L" Input Current 3	I_{IL3}	V_I = 0 V	—	—	–10	μA	DI/O
"L" Input Current 4	I_{IL4}	V_I = 0 V	—	—	–1	μA	OSC1, $\overline{CS}$, $\overline{CP}$,DT, TEST
"L" Input Current 5	I_{IL5}	V_{DD} = 3 V, V_I = 0 V	–4	–10	–25	μA	$\overline{RESET}$
"L" Input Current 6	I_{IL6}	V_{DD} = 3 V, V_I = 0 V	–0.04	–0.1	–0.2	mA	$\overline{C0}$ to $\overline{C4}$
"H" Output Voltage 1	V_{OH1}	I_O = –0.4 mA	V_{DD} – 0.4	—	—	V	DI/O, KREQ
"H" Output Voltage 2	V_{OH2}	I_O = –40 μA	$0.9V_{DD}$	—	—	V	OSC2
"H" Output Voltage 3	V_{OH3}	I_O = –15 mA	V_{DD} – 1.7	—	—	V	PA0, PB5 to PB7
"H" Output Voltage 4	V_{OH4}	I_O = –2 mA	V_{DD} – 1.2	—	—	V	PB0 to PB4
"H" Output Voltage 5	V_{OH5}	I_O = –50 μA	V_{DD} – 2.0	—	—	V	$\overline{R0}$ to $\overline{R4}$
"L" Output Voltage 1	V_{OL1}	I_O = 0.4 mA	—	—	0.4	V	DI/O, KREQ
"L" Output Voltage 2	V_{OL2}	I_O = 40 μA	—	—	$0.1V_{DD}$	V	OSC2
"L" Output Voltage 3	V_{OL3}	I_O = 1 mA	—	—	0.4	V	PA0, PB0 to PB7
"L" Output Voltage 4	V_{OL4}	I_O = 1.8 mA	—	—	0.7	V	$\overline{R0}$ to $\overline{R4}$
Segment Output Voltage 1(1/4 bias)	V_{OS0}	I_O = –10 μA	V_{S2} – 0.6	—	—	V	SEG1 to SEG80
	V_{OS1}	I_O = ±10 μA	$2/4V_{S2}$ – 0.6	—	$2/4V_{S2}$ + 0.6	V	
	V_{OS2}	I_O = ±10 μA	$2/4V_{S2}$ – 0.6	—	$2/4V_{S2}$ + 0.6	V	
	V_{OS3}	I_O = +10 μA	—	—	V_{SS} + 0.6	V	

(V_{DD} = 2.7 to 5.5 V, V_{S2} = 6 to 16 V, Ta = –40 to +85°C)

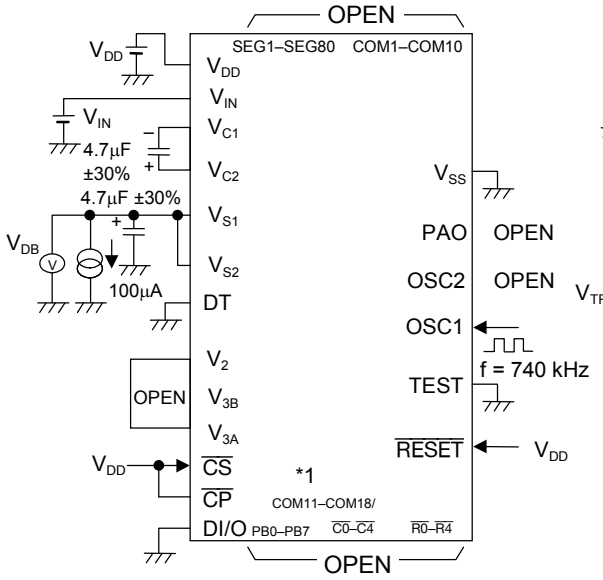
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Pins
Common Output Voltage 1 (1/4 bias)	V_{OC0}	I_O = –10 μA	V_{S2} – 0.3	—	—	V	COM1 to COM18
	V_{OC1}	I_O = ±10 μA	3/4V_{S2} – 0.3	—	3/4V_{S2} + 0.3	V	
	V_{OC2}	I_O = ±10 μA	1/4V_{S2} – 0.3	—	1/4V_{S2} + 0.3	V	
	V_{OC3}	I_O = +10 μA	—	—	V_{SS} + 0.3	V	
Segment Output Voltage 2 (1/5 bias)	V_{OS0}	I_O = –10 μA	V_{S2} – 0.6	—	—	V	SEG1 to SEG80
	V_{OS1}	I_O = ±10 μA	3/5V_{S2} – 0.6	—	3/5V_{S2} + 0.6	V	
	V_{OS2}	I_O = ±10 μA	2/5V_{S2} – 0.6	—	2/5V_{S2} + 0.6	V	
	V_{OS3}	I_O = +10 μA	—	—	VSS+0.6	V	
Common Output Voltage 2 (1/5 bias)	V_{OC0}	I_O = –10 μA	V_{S2} – 0.3	—	—	V	COM1 to COM18
	V_{OC1}	I_O = ±10 μA	4/5V_{S2} – 0.3	—	4/5V_{S2} + 0.3	V	
	V_{OC2}	I_O = ±10 μA	1/5V_{S2} – 0.3	—	1/5V_{S2} + 0.3	V	
	V_{OC3}	I_O = +10 μA	—	—	V_{SS} + 0.3	V	
Voltage Multiplier Voltage 1	V_{DB}	External clock = 740 KHz V_{IN} = 3.55 to 8.0 V 1/4 bias *1	V_{IN} × 1.83 –0.5	15 *6	V_{IN} × 2	V	V_{S2}
Voltage Multiplier Voltage 2	V_{TR}	External clock = 740 KHz V_{IN} = 2.84 to 5.33 V 1/4 bias *2	V_{IN} × 2.46 –1.0	13 *7	V_{IN} × 3	V	V_{S2}
Supply Current 1	I_{DD1}	R = 56KΩ *3	—	—	0.95	mA	V_{DD}
Supply Current 2	I_{DD2}	External clock = 740 KHz *4	—	—	0.7	mA	V_{DD}
Supply Current 3	I_{VIN}	R = 56KΩ *3	—	—	2	mA	V_{IN}
LCD Driving Bias Resistance	LBR	*5	6.3	9	13	kΩ	V_{S2} – V_2, V_2 – V_{3B}, V_{3A} – V_{SS}

*1: Refer to Measuring Circuits 1
*2: Refer to Measuring Circuits 2
*3: Refer to Measuring Circuits 3
*4: Refer to Measuring Circuits 4
*6: V_{IN} = 8 V, Ta = 25°C
*7: V_{IN} = 5.33 V, Ta = 25°C

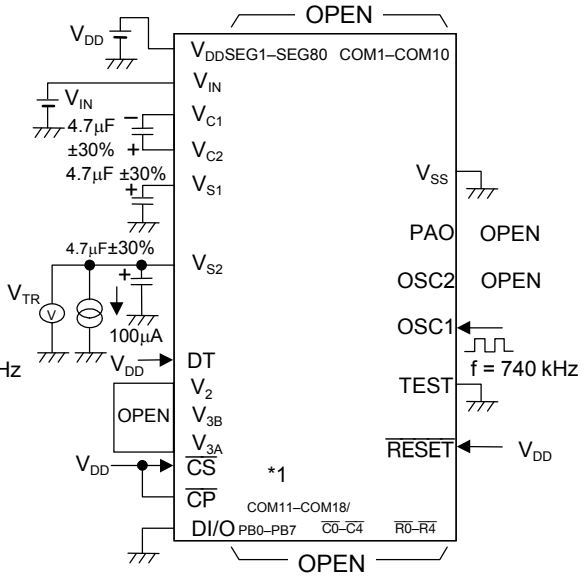


Measuring Circuits

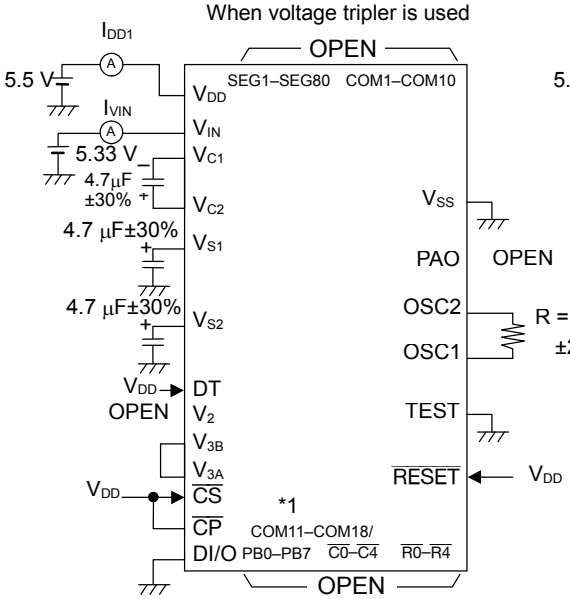
Measuring Circuit 1
Voltage multiplier voltage 1
When voltage doubler is used.
1/4 bias



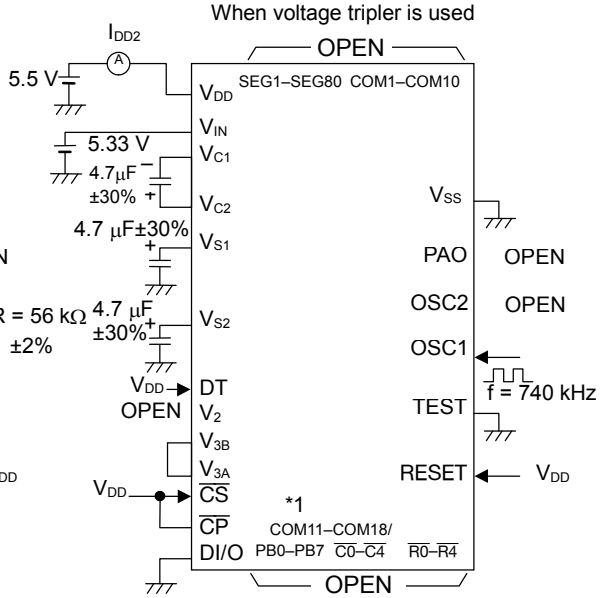
Measuring Circuit 2
Voltage multiplier voltage 2
When voltage tripler is used.
1/4 bias



Measuring Circuit 3
Supply current 1
When voltage tripler is used



Measuring Circuit 4
Supply current 2
When voltage tripler is used



*1: PB0 - PB7 for ML9090A-01, and COM11 - COM18 for ML9090A-02

Switching Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{S2} = 6 to 16 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min	Max	Unit
$\overline{CP}$ Clock Cycle Time	t_{SYS}	—	1000	—	ns
$\overline{CP}$ "H" Pulse Width	t_{WH}	—	400	—	ns
$\overline{CP}$ "L" Pulse Width	t_{WL}	—	400	—	ns
$\overline{CS}$ "H" Pulse Width	t_{WCH}	—	200	—	ns
$\overline{CP}$ Clock Rise/fall Time	t_r, t_f	—	—	100	ns
$\overline{CS}$ Setup Time	t_{CSU}	—	60	—	ns
$\overline{CS}$ Hold Time	t_{CHD}	—	290	—	ns
DI/O Setup Time	t_{DSU}	—	100	—	ns
DI/O Hold Time	t_{DHD}	—	15	—	ns
DI/O Output Delay Time	t_{DOD}	CL = 50 pF	—	200	ns
DI/O Output OFF Delay Time	t_{DOFF}	CL = 50 pF	—	200	ns
$\overline{RESET}$ Pulse Width	t_{WRE}	—	2	—	µs
External Clock Cycle Time	t_{SES}	—	833	—	ns
External Clock "H" Pulse Width	t_{WEH}	—	316	—	ns
External Clock "L" Pulse Width	t_{WEL}	—	316	—	ns
External Clock Rise/fall Time	t_{rE}, t_{fE}	—	—	100	ns

Key Scan Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{S2} = 6 to 16 V, Ta = –40 to +85°C)

Parameter	Symbol	Register setting	Dividing ratio	Oscillation frequency			Unit
		KT		480 kHz	740 kHz	1200 kHz	
Key Scan Cycle	T_{scn}	0	1/3780	7.9	5.1	3.1	ms
		1	1/7560	15.8	10.2	6.2	
Key Scan Invalid Time	T_{nop}	0	1/4800	10.0	6.5	4.0	
		1	1/9600	20.0	13.0	8.0	

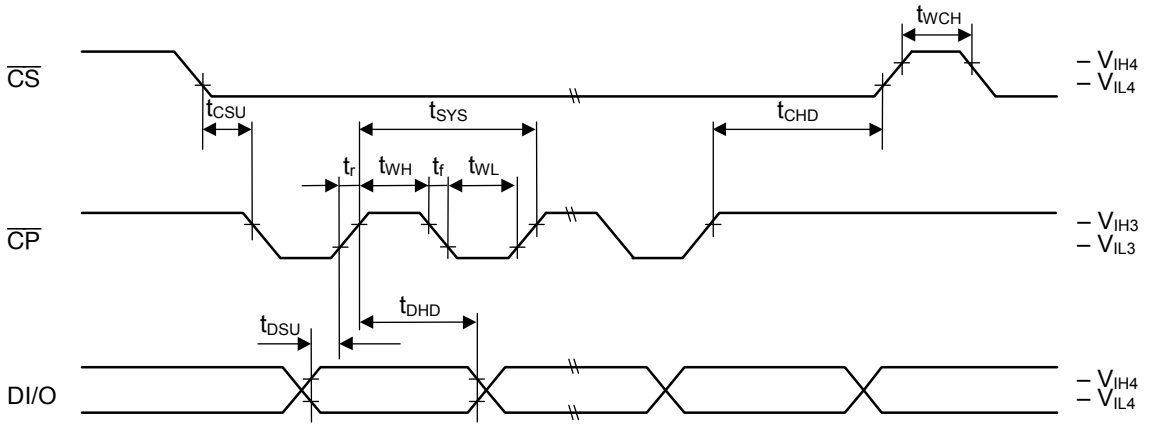
Frame Frequency Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{S2} = 6 to 16 V, Ta = –40 to +85°C)

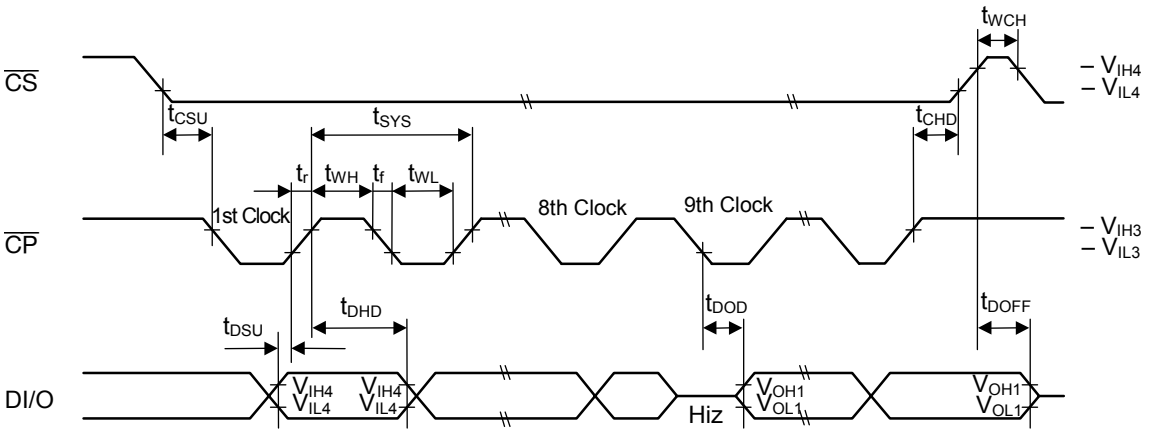
Model	Parameter	Symbol	Display duty	Dividing ratio	Oscillation frequency			Unit
					480 kHz	740 kHz	1200 kHz	
ML9090A-01	Frame Frequency	FRM	1/8	1/6144	78.1	120.4	195.3	Hz
			1/9	1/6912	69.4	107	173.7	
			1/10	1/7680	62.5	96.3	156.3	
ML9090A-02			1/16	1/6144	78.1	120.4	195.3	
			1/17	1/6528	73.5	113.3	183.9	
			1/18	1/6912	69.4	107	173.7	

Clock synchronous serial interface timing diagrams

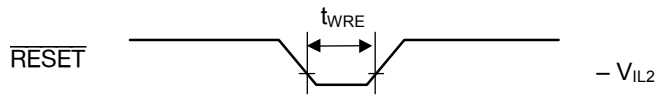
Clock synchronous serial interface input timing



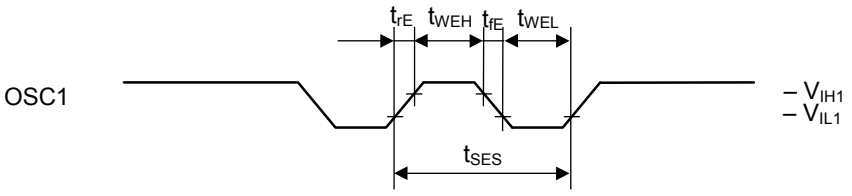
Clock synchronous serial interface input/output timing



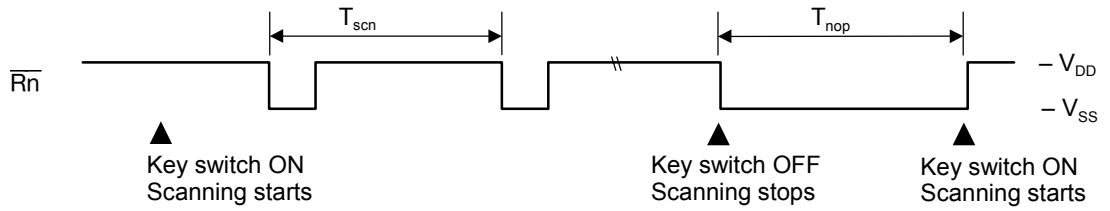
Reset timing



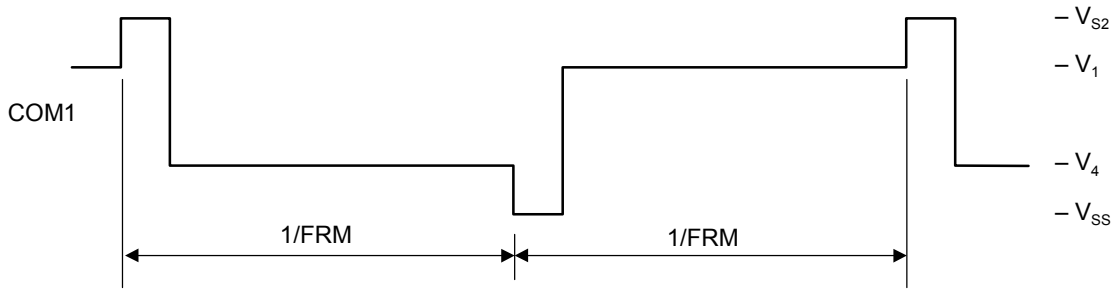
External clock



Key scan timing



Frame frequency



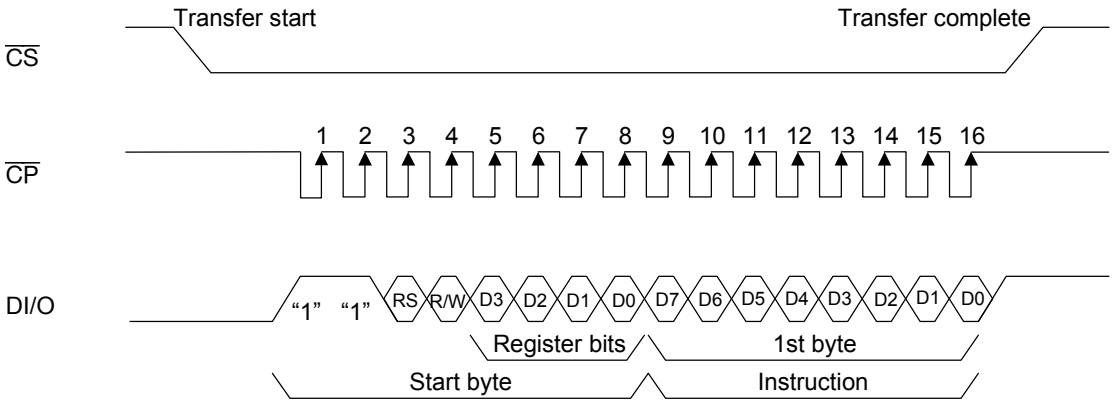
Instruction Code List

Instruction	Start byte								Instruction code								Descriptions
	Fixed bit		RS	R/W	Register No.				D7	D6	D5	D4	D3	D2	D1	D0	
	D7	D6	D5	D4	D3	D2	D1	D0									
Key scan register read	1	1	0	1	0	0	0	0	ST2	ST1	ST0	S4	S3	S2	S1	S0	Reads scan read count display bits (ST0 to ST2) and key scan data (S0 to S4) of the key scan register.
Display data RAM write	1	1	1	0	0	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0	Writes display data (D0 to D7) in the display data RAM after setting the X address or Y address.
Display data RAM read	1	1	1	1	0	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0	Reads display data (D0 to D7) from the display data RAM after setting the X address or Y address.
X address register set	1	1	0	0	0	0	1	0	—	—	—	—	X3	X2	X1	X0	Sets the X address (X0 to X3) of the display data RAM.
Y address register set	1	1	0	0	0	0	1	1	—	—	—	Y4	Y3	Y2	Y1	Y0	Sets the Y address (Y0 to Y4) of the display data RAM.
Port register A set	1	1	0	0	0	1	0	0	—	—	—	—	—	—	—	PTA	Controls the output of the general-purpose port A (PTA).
Port register B set	1	1	0	0	0	1	0	1	PTB7	PTB6	PTB5	PTB4	PTB3	PTB2	PTB1	PTB0	Controls the output of the general-purpose port B (PTB0 to PTB7).
Control register 1 set	1	1	0	0	1	0	0	0	INC	WLS	KT	SHL	—	—	DTY1	DTY0	Sets the address increment X or Y direction (INC), display data word length (WLS), key scan time (KT), common driver shift direction (SHL), and display duty (DTY0, DTY1).
Control register 2 set	1	1	0	0	1	0	0	1	—	—	T4	T3	T2	T1	—	DISP	Sets test mode (T1 to T4) and display ON/OFF (DISP).

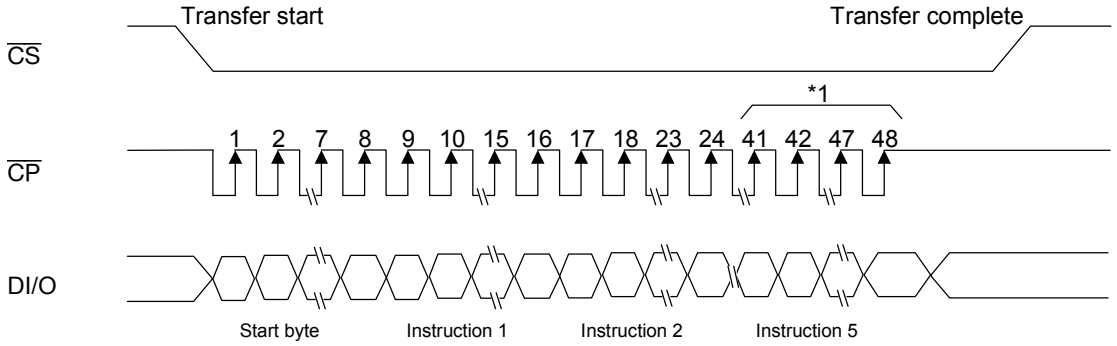
RS : Register select bit 1: RAM 0: Register
R/W : Read/write select bit 1: Read 0: Write
ST0 to ST2 : Key scan read count display bits
S0 to S4 : Key scan data
D0 to D7 : Write or read data of the display data RAM
X0 to X3 : X address of the display data RAM
Y0 to Y4 : Y address of the display data RAM
PTA : Port A data
PTB0 to PTB7 : Port B data (ML9090A-01 only)
INC : Display data RAM address increment 1 : X direction, 0: Y direction

WLS : Word length select bit 1: 6 bits, 0: 8 bits
KT : Key scan cycle select bit 1: 10 ms, 0: 5 ms
DTY0, DTY1 : Display duty select bit (1/8, 1/9, 1/10) (ML9090A–01)
(1/16, 1/17, 1/18) (ML9090A–02)
SHL : Common driver shift direction select bit
1: COM10 → COM1, 0: COM1 → COM10 (ML9090A-01)
1: COM18 → COM1, 0: COM1 → COM18 (ML9090A-02)
DISP : Display ON/OFF select bit 1: Display ON, 0: Display OFF
T1 to T4 : Write “0” to use for test mode
— : Don't Care

Clock Synchronous Serial Transfer Example (WRITE)

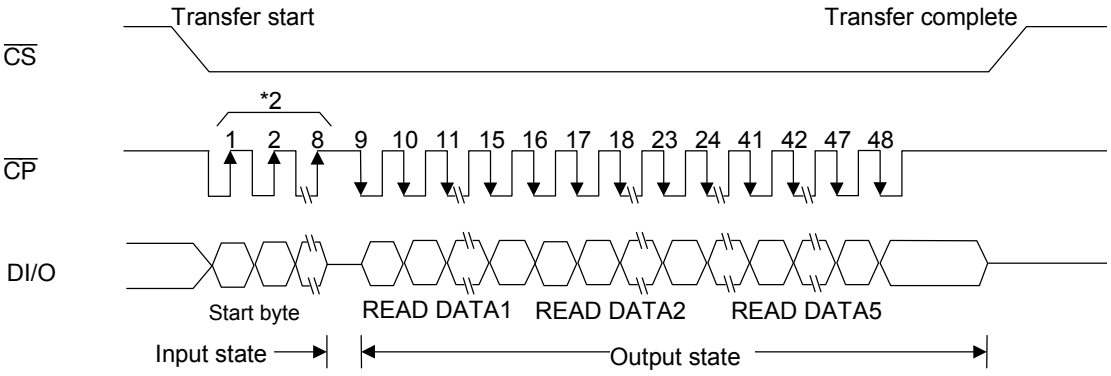


Clock Synchronous Serial Continuous Data Transfer Example (WRITE)



*1: Write data in 8 bits. If the $\overline{CS}$ signal falls when data input operation in 8 bits is not complete, the last 8-bit data write is invalid.
(The previously written data is valid)

Clock Synchronous Serial Continuous Data Transfer Example (READ)



*2: A reading state appears only when the R/W bit is "1". The read data is valid only when the register is set to key scan read mode and display data read mode. Otherwise, the read data is invalid.

Output pin, I/O Pin and Register States When Reset is Input

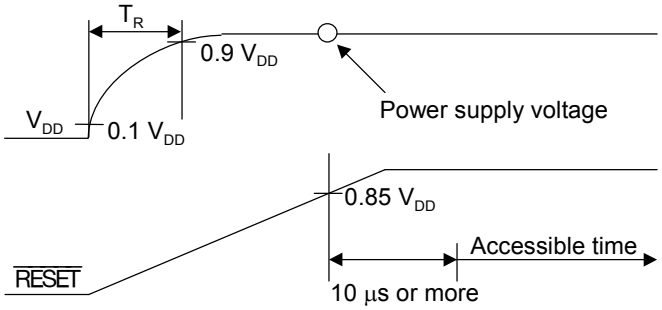
Pin and register states while the $\overline{\text{RESET}}$ input is pulled to a "L" level are listed below.

Output pin, I/O pin	State
DI/O	Input state
KREQ	"L" (V_{SS})
OSC2	Oscillating state
$\overline{R0}$ to $\overline{R4}$	"L" (V_{SS})
PBA	High impedance
PB0 to PB7 (for ML9090A-01)	High impedance
SEG1 to SEG80	"L" (V_{SS})
COM1 to COM10 (for ML9090A-01)	"L" (V_{SS})
COM1 to COM18 (for ML9090A-02)	"L" (V_{SS})

Register	State
Key scan register	Reset to "0"
Display data register	Display data is retained
X address register	Reset to "0"
Y address register	Reset to "0"
Port A register	Reset to "0"
Port B register	Reset to "0"
Control register 1	No change from value prior to reset input
Control register 2	Display OFF

Power-On Reset

The capacitance of an external capacitor that is connected to the $\overline{\text{RESET}}$ pin must be C_{RST} [μF] ≥ 12.5 × T_R [s], where T_R is rise time until power supply voltage to be supplied to the ML9090A-01/02 reaches 0.8 V_{DD} (V) and C_{RST} is the capacitance of an external capacitor connected to the $\overline{\text{RESET}}$ pin.
(If T_R = 10 [ms], C_{RST} ≥ 0.125 [μF])
The pulse width when an external reset signal is input should be more than T_R.
Set an instruction 10 μs after the reset signal is released.
Thereafter, this IC is accessible.



Serial Interface Operation

1. Start byte

A register that transfers instruction codes (including display data or key scan data) is selected by a content of the start byte (see below).

D7	D6	D5	D4	D3	D2	D1	D0
"1"	"1"	RS	R/W	Register number			

(1) D7, D6 (fixed at "1")
When selecting the start byte register, always write a "1" to bits D7 and D6.

(2) D4 (R/W) (Read mode, Write mode select bit)
1: Read mode is selected
0: Write mode is selected

(3) D5, D3 to D0 (Register number)
The correspondence between each content of the start byte and each register or the display data RAM is listed in the table below.

D7	D6	D5	D4	D3	D2	D1	D0	Register name
1	1	0	1	0	0	0	0	Key scan register
1	1	1	1/0	0	0	0	1	Display data RAM
1	1	0	0	0	0	1	0	X address register
1	1	0	0	0	0	1	1	Y address register
1	1	0	0	0	1	0	0	Port A register
1	1	0	0	0	1	0	1	Port B register
1	1	0	0	1	0	0	0	Control register1
1	1	0	0	1	0	0	1	Control register 2

Register Descriptions

- Key scan register (KR)

D7	D6	D5	D4	D3	D2	D1	D0
ST2	ST1	ST0	S4	S3	S2	S1	S0

(1) D7 to D5 (ST2 to ST0) (Scan read counter)
When reading 25-bit key scan data, these bits indicate the number of times scan data has been read. Every time key scan data is read, these bits (ST2 to ST0) are automatically incremented over the range of "000" to "100". After counting to "100", this key scan data read counter is reset to "000".
If the $\overline{\text{RESET}}$ pin is pulled to a "L" level, these bits are reset to "0".

(2) D4 to D0 (S4 to S0) (Key scan read data bits)
These bits are read as 25-bit serial data that expresses the key switch status (1 = ON, 0 = OFF). Data is divided into 5 groups and read. (For the read order, refer to the description below.) The read count is indicated by bits ST2 to ST0. S4 to S0 key scan data corresponds to each SWN0 of the key matrix shown in figure 1. The relation between the key scan data, key matrix signal and each SWN0 of the key matrix is shown below.
If the $\overline{\text{RESET}}$ pin is pulled to a "L" level, these bits are reset to "0".

ST2	ST1	ST0	S4	S3	S2	S1	S0	
0	0	0	SW04	SW03	SW02	SW01	SW00	$\overline{R0}$
0	0	1	SW14	SW13	SW12	SW11	SW10	$\overline{R1}$
0	1	0	SW24	SW23	SW22	SW21	SW20	$\overline{R2}$
0	1	1	SW34	SW33	SW32	SW31	SW30	$\overline{R3}$
1	0	0	SW44	SW43	SW42	SW41	SW40	$\overline{R4}$

(Note) SW00 to SW44 swithes are shown in Figure1.

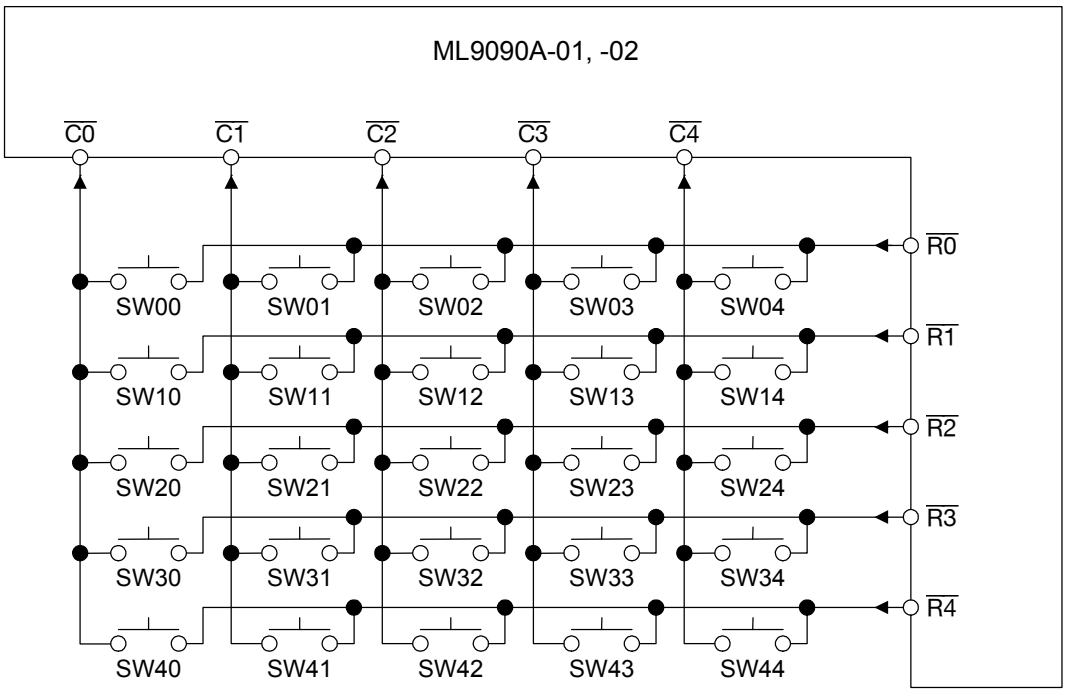
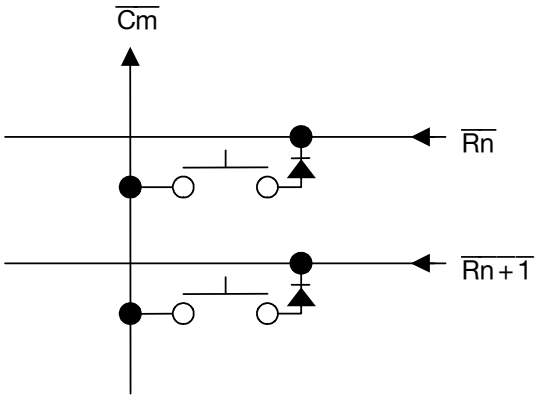


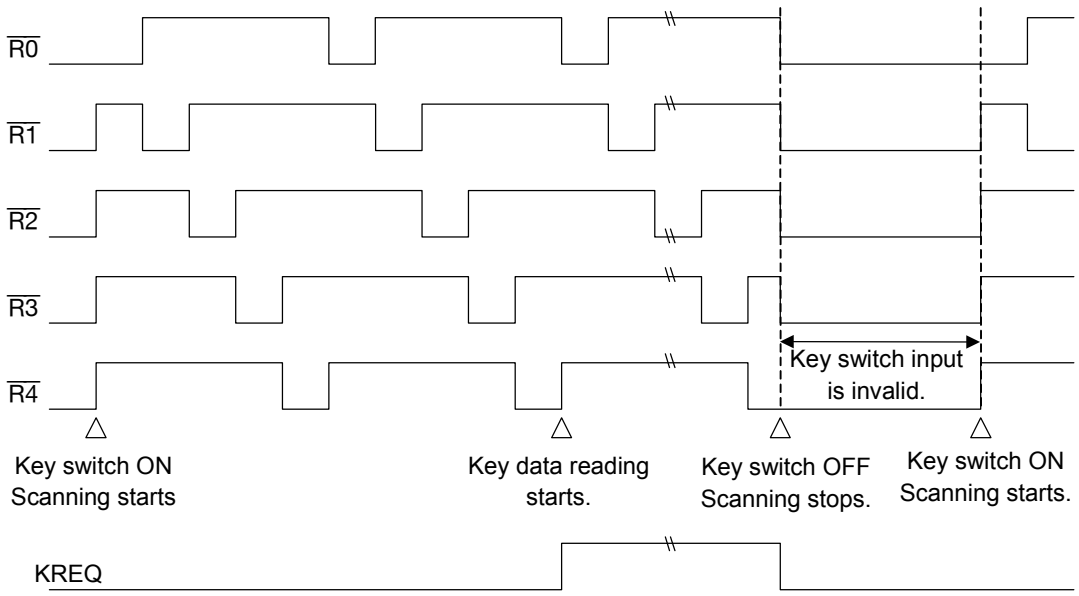
Figure 1

(Note) To recognize simultaneous depression of three or more key switches, add a diode in series to each key.



Key Scan

The key scanning starts when a key switch is pressed on and ends after all key switches are detected to be off. The KREQ signal changes from the low level "L" to the high level "H" two cycles after key scanning started.
This signal can be used as a flag. To use it as a flag, start key-scan reading when the KREQ signal changes from "L" to "H".
In some cases, scanned data may be unstable if key scan reading starts when the level of the KREQ signal changes from "H" to "L". To avoid this, repeat the key-scan reading three times.
All key switch inputs are inhibited for about 1.26 cycle after all key switches are detected to be off while the KREQ signal is at the "H" level.
The KREQ signal is reset when all key switches are detected to be off or when a low-level signal is applied to the $\overline{\text{RESET}}$ pin.



Note 1: When three or more key switches are pressed at the same time, the ML9090A-01/02 may recognize that an unpressed key switch is pressed. Therefore, to recognize simultaneous depression of three or more key switches, add a diode in series to each key. (See Figure 1.) To ignore simultaneous depression of three or more key switches, a program may be required to ignore all key data which contain three or more consecutive "1" values.

- Display data RAM (DRAM)

D7	D6	D5	D4	D3	D2	D1	D0
8-bit DATA							
—	6-bit DATA						

The display data register writes and reads display data to and from the liquid crystal display RAM. The contents of this register are written to or read from the address set by the X address register and Y address register. The bit length of display data can be selected by the WLS bit of control register 1. If 6-bit data has been selected, writing to D7 and D6 is invalid, and if read, their values will always be "0". D7 is the MSB (D5 in the case of 6-bit data) and D0 is the LSB.
The X address and Y address should be set immediately before writing or reading display data. However, only one-time settings of X address and Y address are required immediately before successive writings or readings. Either X address or Y address may be set first.
Even if the $\overline{\text{RESET}}$ pin is pulled to a "L" level, the contents of this register will not change.

- X address register (XAD)

D7	D6	D5	D4	D3	D2	D1	D0
—				XAD			

The X address register sets the X address for the liquid crystal display RAM.
The address setting range is 0 to 9 (00H to 09H) when 8-bit data is selected by the WLS bit. This register starts counting up from the set value each time RAM is read or written.
When the register count returns to 0 from the maximum value 9, the Y address is automatically incremented.
Thereafter, the Y address is counted in a loop fashion from 0 to 9.
The address setting range is 0 to 13 when 6-bit data is selected.
This register starts counting up from the set value. When the register count returns to 0 from 13, theY address is automatically incremented.
Thereafter, the Y address loops from 0 to 13.
Proper operation is not guaranteed if values outside this range are set.
Writing to bits D7 through D4 is invalid. If the $\overline{\text{RESET}}$ pin is pulled to a "L" level, these bits are reset to "0".

- Y address register (YAD)

D7	D6	D5	D4	D3	D2	D1	D0
—				YAD (ML9090A-01)			
—			YAD (ML9090A-02)				

The YAD register sets a Y address of RAM for the liquid crystal display.
The Y address setting range varies according to the setting of the DTY bits (bits D1 and D0) of the control register 1 (to be described later).
This register starts counting up from the set value each time RAM is read or weitten. When the register count returns to 0 from the maximum value (7 to 17), the X address is also incremented automatically.
The Y address is counted in a loop fashion as shown below.

Model	Duty	Y register setting range and loop range	Invalid addres setting range
ML9090A-01	1/8	0 to 7 (00H to 07H)	8 to 15 (08H to FH)
	1/9	0 to 8 (00H to 08H)	9 to 15 (09H to FH)
	1/10	0 to 9 (00H to 09H)	10 to 15 (AH to FH)
ML9090A-02	1/16	0 to 15 (00H to 0FH)	16 to 31 (10H to 1FH)
	1/17	0 to 16 (00H to 10H)	17 to 31 (11H to 1FH)
	1/18	0 to 17 (00H to 11H)	18 to 31 (12H to 1FH)

When an invalid Y address is set, counting of invalid Y addresses varies according to the selected duty although its operation is not assured. In case the duty is 1/8 or 1/16, the register counts up to a maximum invalid Y address value (15 for the ML9090A-01 or 31 for the ML9090A-02) and back to 0. At the same time, the X address is also incremented.
In case the duty is 1/9 or 1/17, the register counts back to 0 at address "Y address setting plus 1" after an invalid Y address is set. At the same time, the X address is also incremented.
In case the duty is 1/10 or 1/18, the register counts back to 0 at address "Y address setting plus 1" and at address "Y address setting plus 1" after an invalid Y address is set. At the same time, the X address is also incremented. After this, the Y address count loops in a range corresponding to the selected duty.
Both read and write operations on bits D7 to D4 of the ML9090A-01 are invalid.
Both read and write operations on bits D7 to D5 of the ML9090A-02 are invalid.
This register is reset to "0" when the $\overline{\text{RESET}}$ pin is made low.

- Port register A (PTA)

D7	D6	D5	D4	D3	D2	D1	D0
—							PTA

The port register A sets (to "1") and resets (to "0") general-purpose port A data. The setting of the PTA bit (D0 bit) corresponds to the PA0 output pin. If the $\overline{\text{RESET}}$ pin is pulled to a "L" level, this register is reset to "0" and the PA0 pin goes to high impedance. After the $\overline{\text{RESET}}$ pin is pulled to a "H" level, if port data is set in this register, the PA0 pin is released from its high impedance state and outputs the corresponding port data.

- Port register B (PTB)

D7	D6	D5	D4	D3	D2	D1	D0
PTB7	PTB6	PTB5	PTB4	PTB3	PTB2	PTB1	PTB0

The port register sets (to "1") and resets (to "0") general-purpose port B data. The settings of the PTB0 to PTB7 bits (D0 to D7 bits) correspond to the PTB0 to PTB7 output pins. If the $\overline{\text{RESET}}$ pin is pulled to a "L" level, this register is reset to "0" and pins PTB0 through PTB7 go to high impedance. After the $\overline{\text{RESET}}$ pin is pulled to a "H" level, if port data is set in this register, pins PTB0 through PTB7 are released from their high impedance states and output the corresponding port data.

- Control register 1 (FCR1)

D7	D6	D5	D4	D3	D2	D1	D0
INC	WLS	KT	SHL	—	—	DTY1	DTY0

(1) D7 (INC) Address increment direction
1: X direction address increment
0: Y direction address increment
This bit sets the address increment direction of the display RAM. The display RAM address is automatically incremented by 1 every time data is written to the display data register. Writing a "1" to this bit sets "X address increment", and writing a "0" sets "Y address increment". For further details regarding address incrementing, refer to the page entitled "X, Y Address Counter Auto Increment", Even if the $\overline{\text{RESET}}$ pin is pulled to a "L" level, the value of this bit will not change.

(2) D6 (WLS) (Word Length Select)
1: 6-bit word length select
0: 8-bit word length select
This bit selects the word length of data to be written to and read from the display RAM. If "1" is written to this bit, data will be read from and written to the display RAM in 6-bit units. If "0" is written to this bit, data will be read from and written to the display RAM in 8-bit units. Even if the $\overline{\text{RESET}}$ pin is pulled to a "L" level, the value of this bit will not change.

(3) D5 (KT) (Key scan time) Key scan time select bit
1: 10 ms
0: 5 ms
This bit selects the key scan cycle time. In the case of a 740 kHz oscillating frequency, writing a "1" to this bit sets the key scan cycle time at 10 ms, writing a "0" sets the key scan cycle time at 5 ms. Even if the $\overline{\text{RESET}}$ pin is pulled to a "L" level, the value of this bit will not change.

(4) D4 (SHL) (Common driver shift direction select bit)
This bit selects the shift direction of common drivers.
The relationship between this bit and shift directions are shown below.
Even if the $\overline{\text{RESET}}$ Pin is set to "L", this bit remains unchanged.

Model	SHL	Duty	Shift direction
ML9090A-01	1	1/8	COM8 → COM1
		1/9	COM9 → COM1
		1/10	COM10 → COM1
	0	1/8	COM1 → COM8
		1/9	COM1 → COM9
		1/10	COM1 → COM10
ML9090A-02	1	1/16	COM16 → COM1
		1/17	COM17 → COM1
		1/18	COM18 → COM1
	0	1/16	COM1 → COM16
		1/17	COM1 → COM17
		1/18	COM1 → COM18

(5) D1, D0 (DTY1, DTY0) (Display duty select bit)

This bit selects the display duty. The correspondence between each bit and display duty is shown in the chart below. Even if the $\overline{\text{RESET}}$ pin is pulled to a "L" Level, the values of these bits will not change.

Model	Code	DTY1	DTY0	Display duty
ML9090A-01	0	0	0	1/8
	1	0	1	1/9
	2	1	0	1/10
	3	1	1	1/10
ML9090A-02	0	0	0	1/16
	1	0	1	1/17
	2	1	0	1/18
	3	1	1	1/18

- Control register 2 (FCR2)

D7	D6	D5	D4	D3	D2	D1	D0
—		T4	T3	T2	T1	—	DISP

(1) D2 to D5 (T1 to T4) (Test mode select bit)
These bits are used to test the IC. "0" must be written to these bits.

(2) D0 (DISP) (Display ON/OFF mode bit)
1: Display ON mode
0: Display OFF mode

This bit selects whether the display is ON or OFF. Writing a "1" to this bit selects the display ON mode. Writing a "0" to this bit selects the display OFF mode. At this time, the COM and SEG pins will be at the VSS level. Even if this bit is set to "0", the display RAM contents will not change. If the $\overline{\text{RESET}}$ pin is pulled to a "L" level, this register is reset to "0".

Display Screen and Memory Address Allocation

The ML9090A-01/02 contains display data RAM (80 bits by 18 bits) of a bitmap type.
The allocation of memory addresses varies according to the selected word length (6 bits or 8 bits) as shown in Figure 2: 0 to 9 for selection of 8 bits per word or 0 to 13 for selection of 6 bits per word.
The X address 13 in the 6-bits/word mode has two display memory bits. The two bits (D5 and D4) starting from bit D5 of the display data register are written in memory and the other bits (D3 to D0) are ignored.

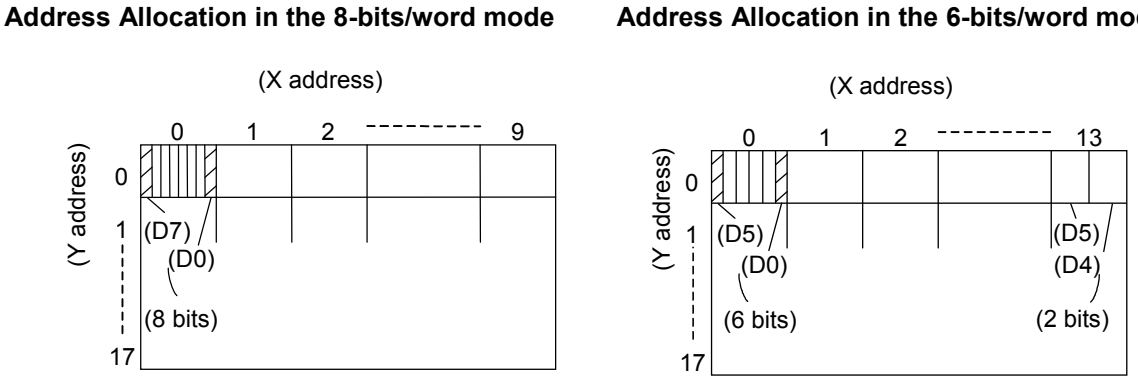


Figure 2 Display Memory Addresses

In the 8-bits/word mode, data to be displayed is written in display memory with the D7 data of the display data register at address (Xn, Yn) and the D0 data at address (Xn + 7, Yn). Similarly, In the 6-bits/word mode, data to be displayed is written in display memory with the D5 data of the display data register at address (Xn, Yn) and the D0 data at address (Xn + 5, Yn). See Figure 3.
Data "1" in display memory represents turning on the corresponding display segment and data "0" in display memory represents turning off the corresponding display segment.

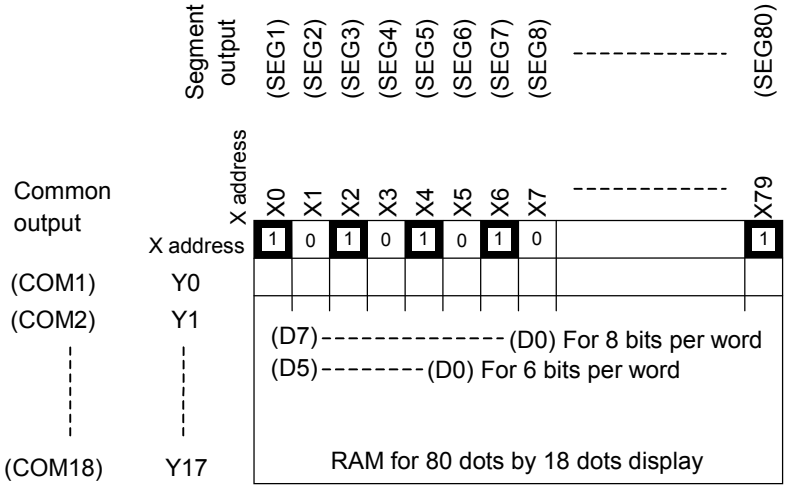


Figure 3 Display Screen Bit Allocation and Memory Addresses

X·Y address Counter Auto Increment

The liquid crystal display RAM for the ML9090A-01/02 has an X-address counter and a Y-address counter. Each address counter has an Auto Increment function.
When display data is read or written, this function increments either of these X- and Y-address counters (which is selected by the INC bit (D7 bit) of the control register 1).

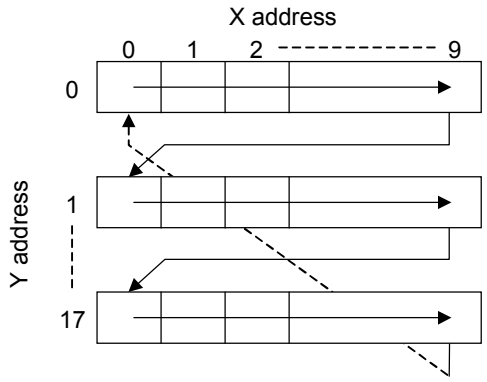
INC bit = "0" selects the Y-address counter.
INC bit = "1" selects the X-address counter.

The address counting cycle of the X address counter varies according to the selected word length (8 bits or 6 bits) : X address range of 0 to 9 in the 8-bits/word mode or X address range of 0 to 13 in the 6-bits/word mode.
When the X address count returns to 0 from a maximum value (9 in the 8-bits/word mode or 13 in the 6-bits/word mode), the Y address is also incremented automatically.
The relationship between display duties and Y address count ranges is shown below.
When the Y-address counter returns to 0 from a maximum value, the X address is also incremented automatically.

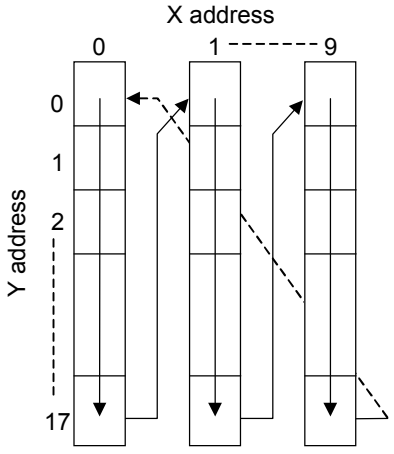
Model	Duty	Y-address count range (cycle)	Maximum Y address count
ML9090A-01	1/8	0 to 7	7
	1/9	0 to 8	8
	1/10	0 to 9	9
ML9090A-02	1/16	0 to 5	15
	1/17	0 to 16	16
	1/18	0 to 17	17

Note: If an invalid address (outside the address count range) is given to the X- or Y- address counter, its counting will not be assured.

Example of incrementing the X-address
(8 bits per word and 1/18 duty)

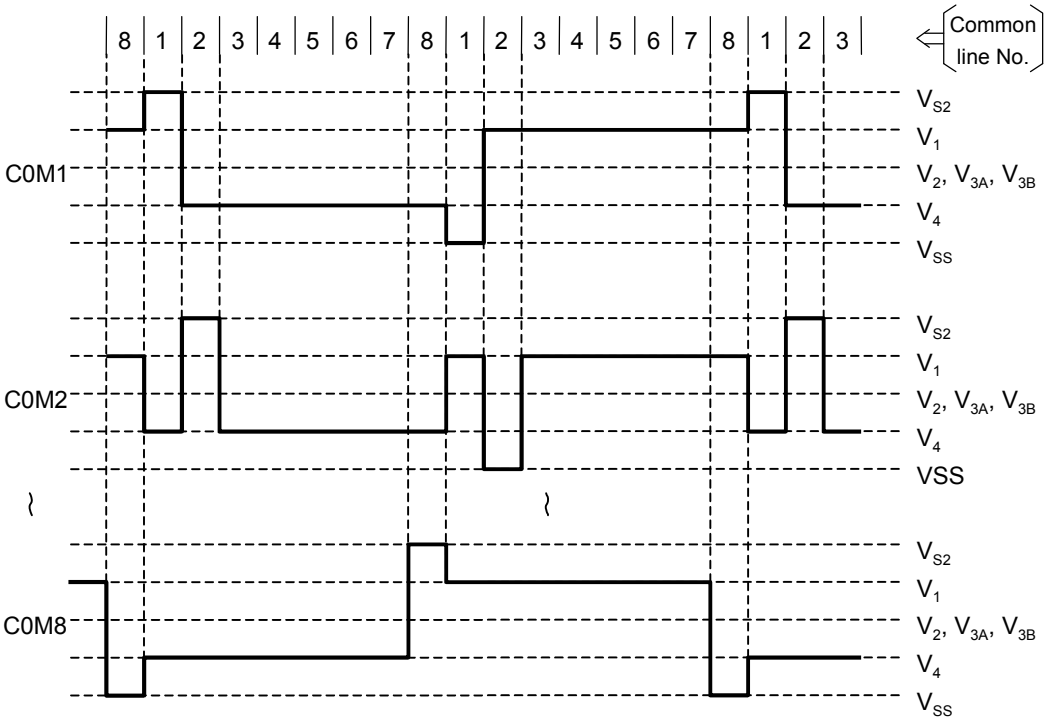


Example of incrementing the Y-address
(8 bits per word and 1/18 duty)

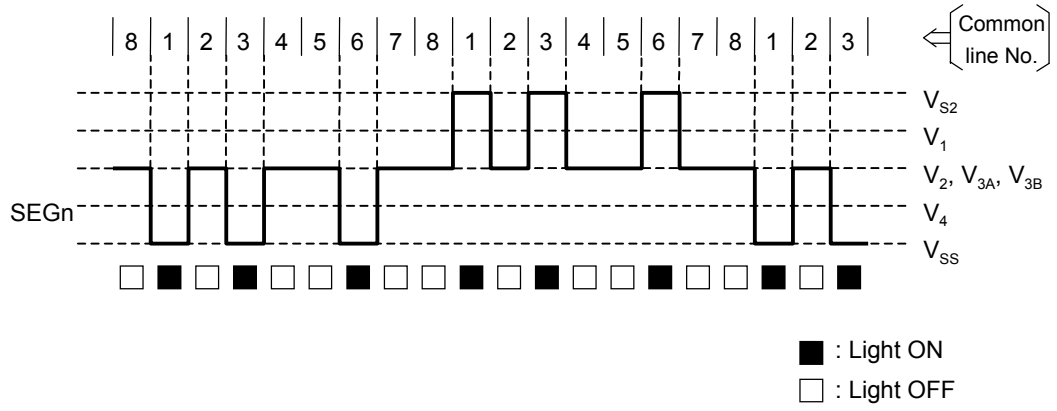


Liquid Crystal Driving Waveform Example (1)

1/8 duty (1/4 bias) (ML9090A-01)

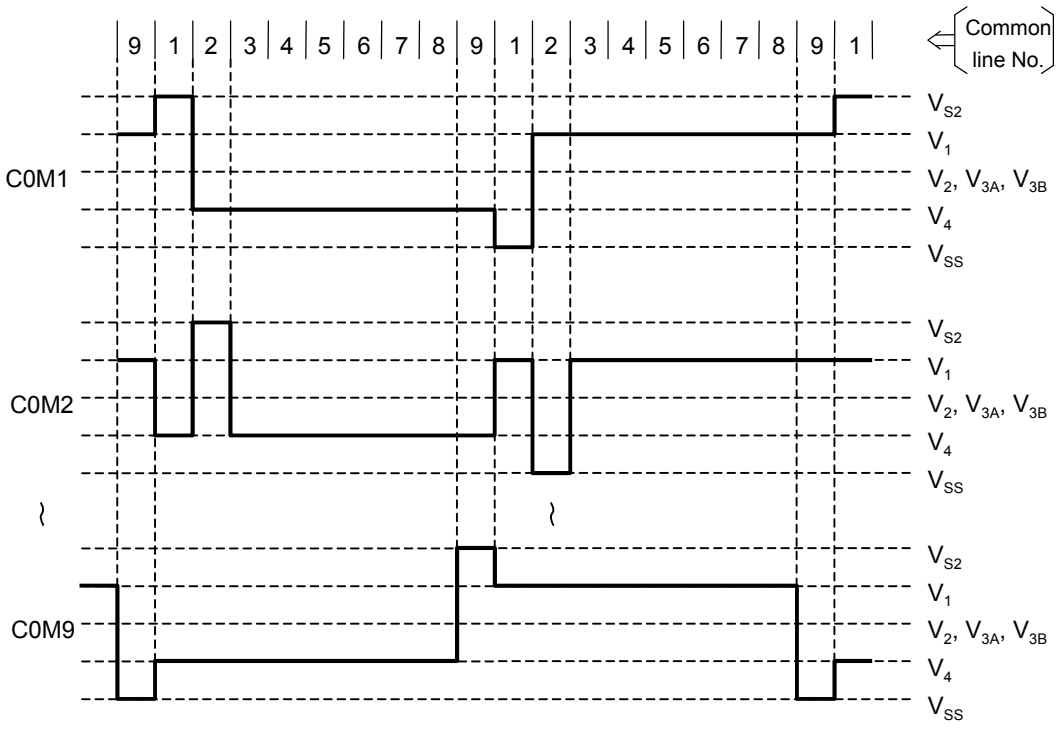


A non-selectable waveform is output from COM9 and COM10 outputs.

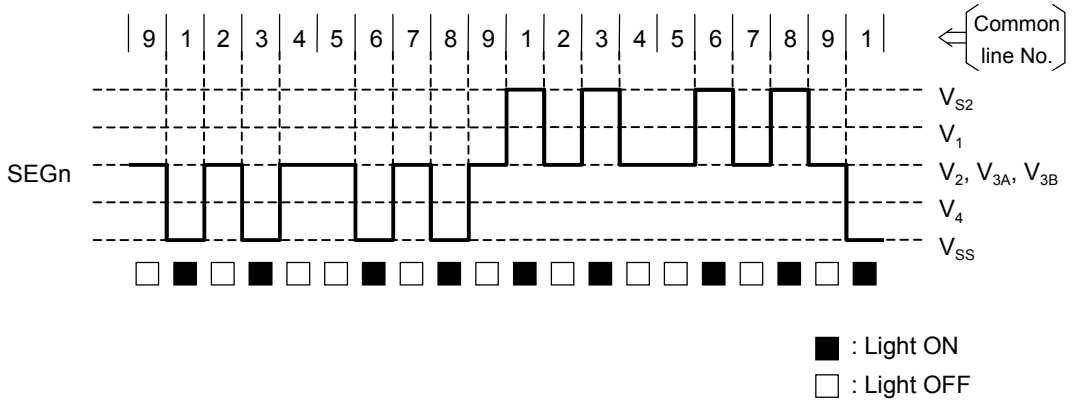


Liquid Crystal Driving Waveform Example (2)

1/9 duty (1/4 bias) (ML9090A-01)

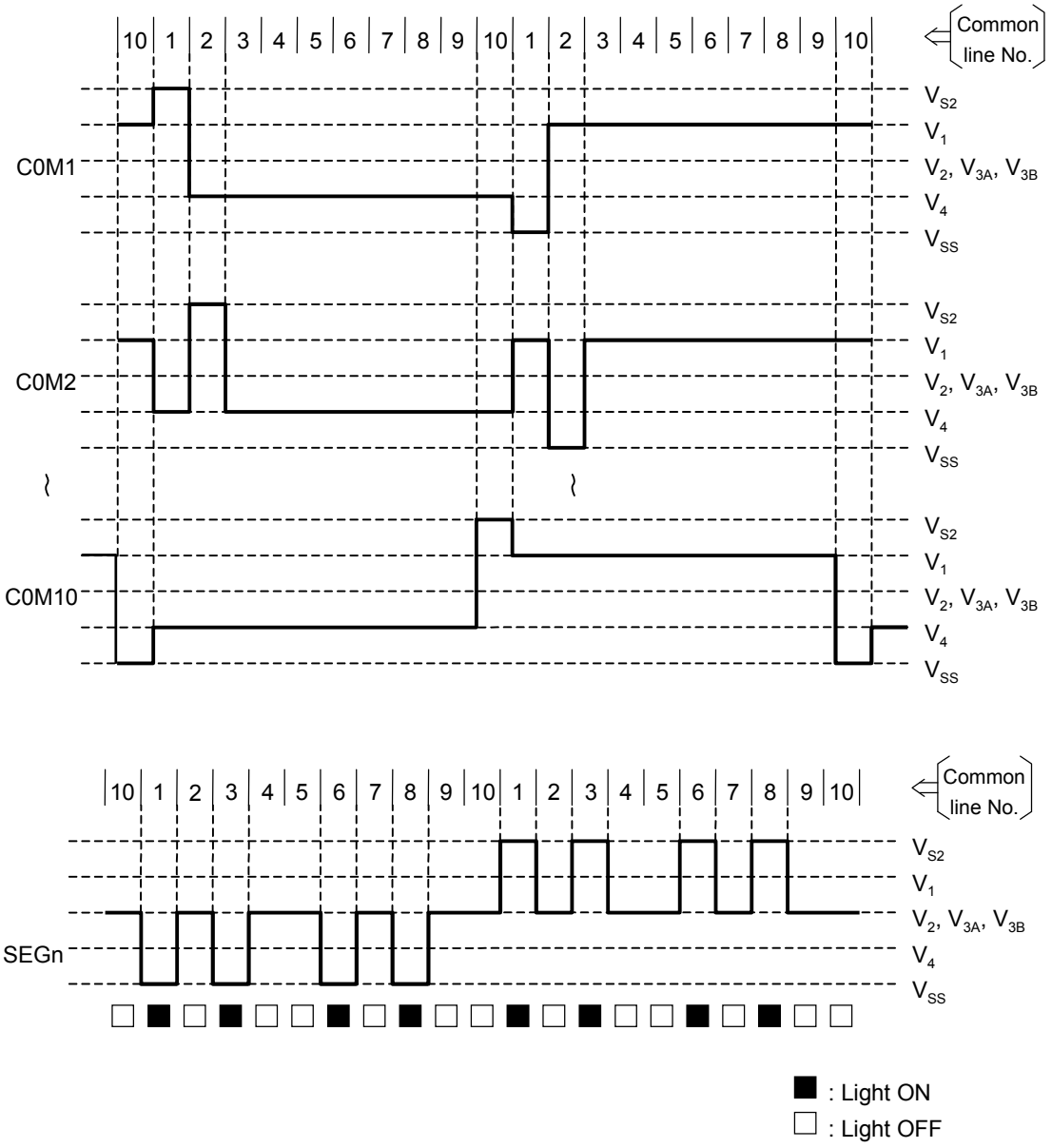


A non-selectable waveform is output from the COM10 output.



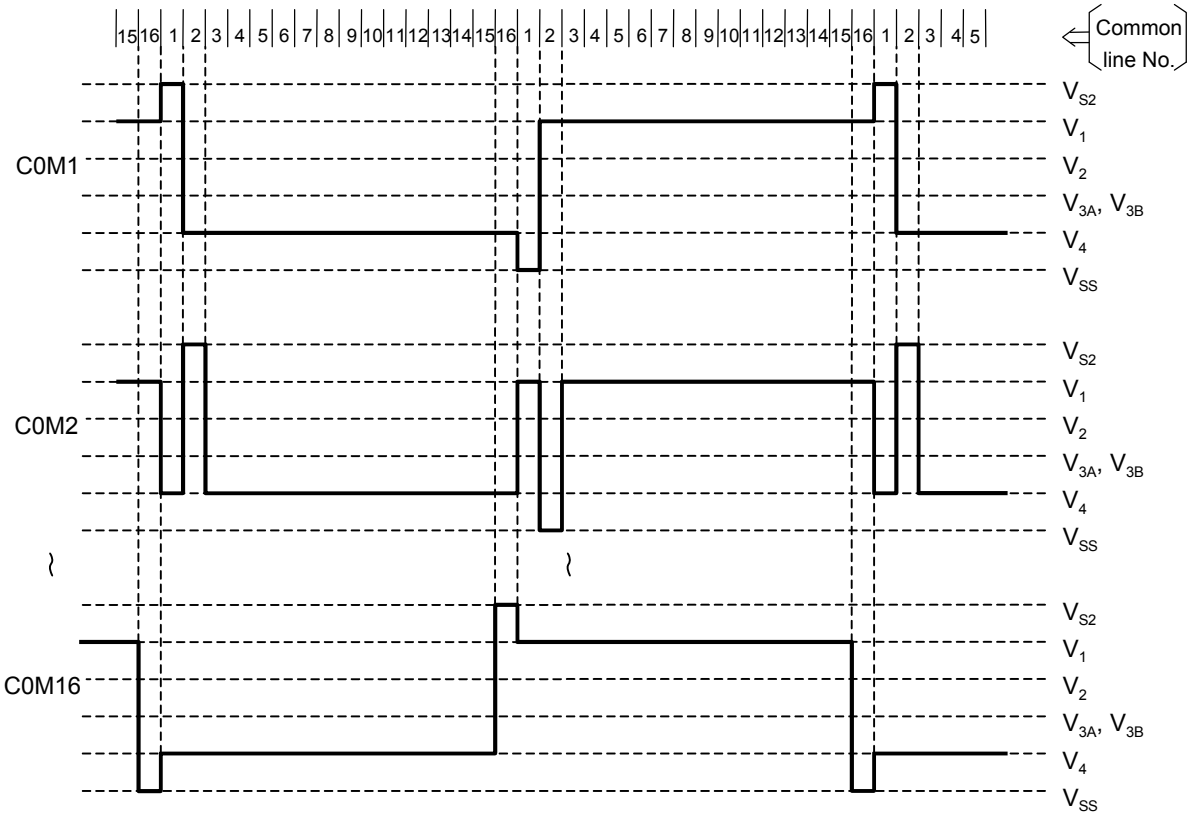
Liquid Crystal Driving Waveform Example (3)

1/10 duty (1/4 bias) (ML9090A-01)

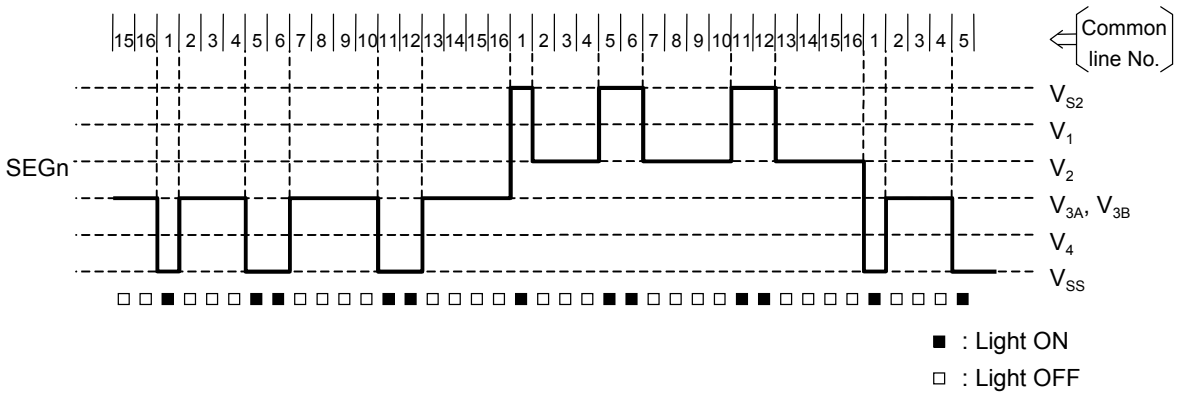


Liquid Crystal Driving Waveform Example (4)

1/16 duty (1/5 bias) (ML9090A-02)

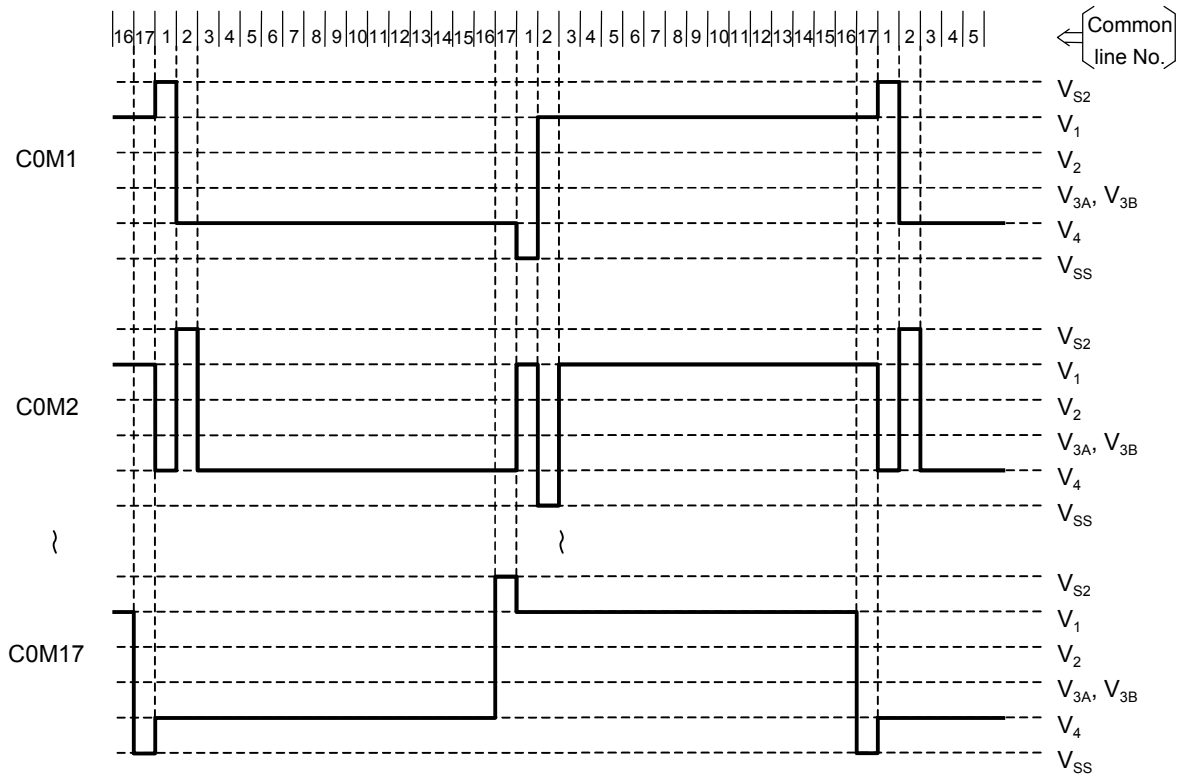


A non-selectable waveform is output from COM17 and COM18 outputs.

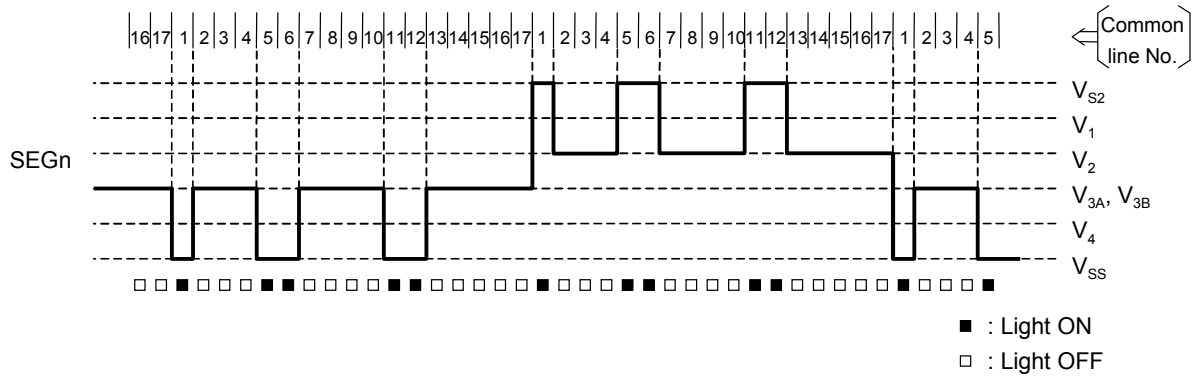


Liquid Crystal Driving Waveform Example (5)

1/17 duty (1/5 bias) (ML9090A-02)

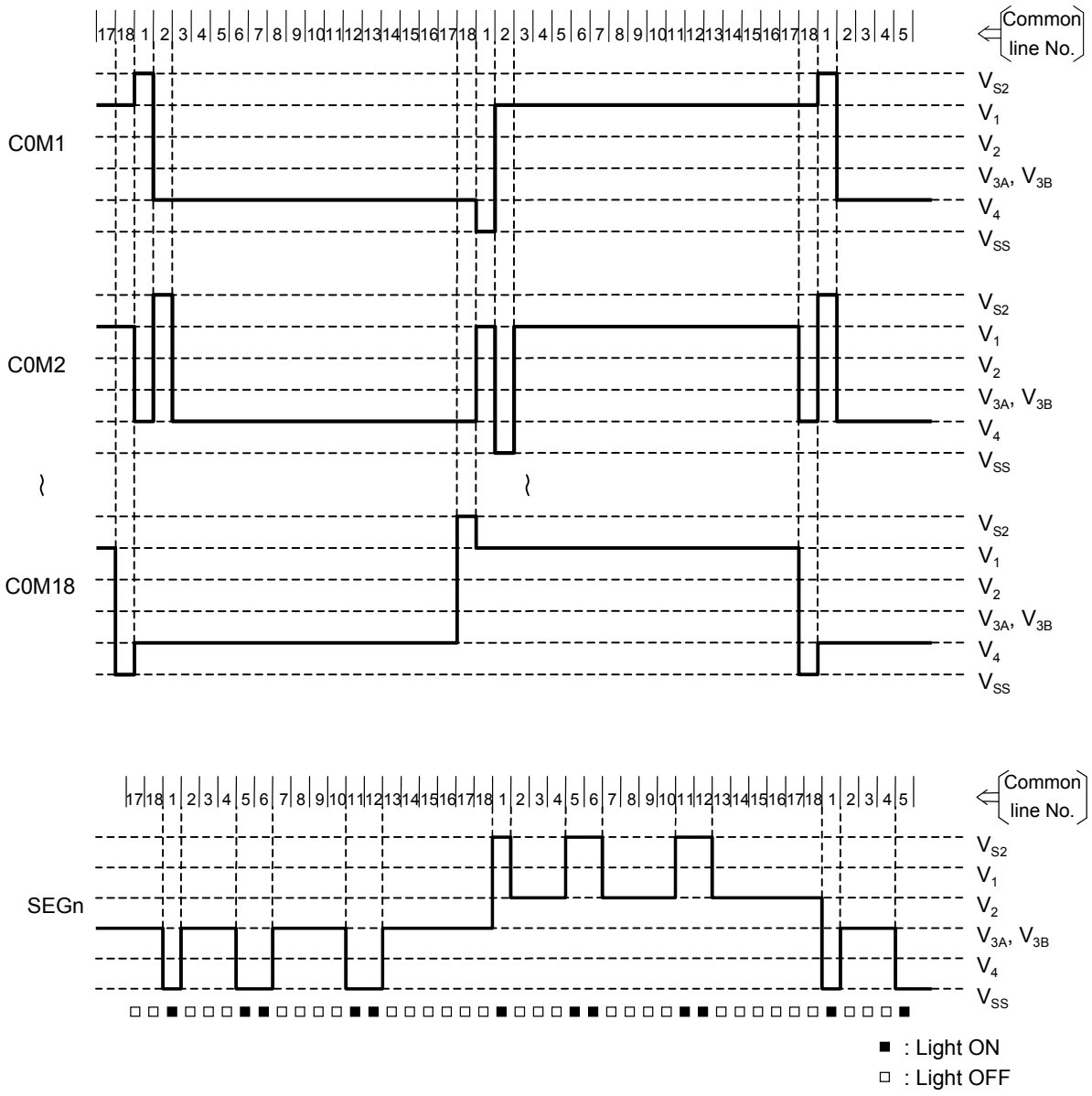


A non-selectable waveform is output form the COM18 output.

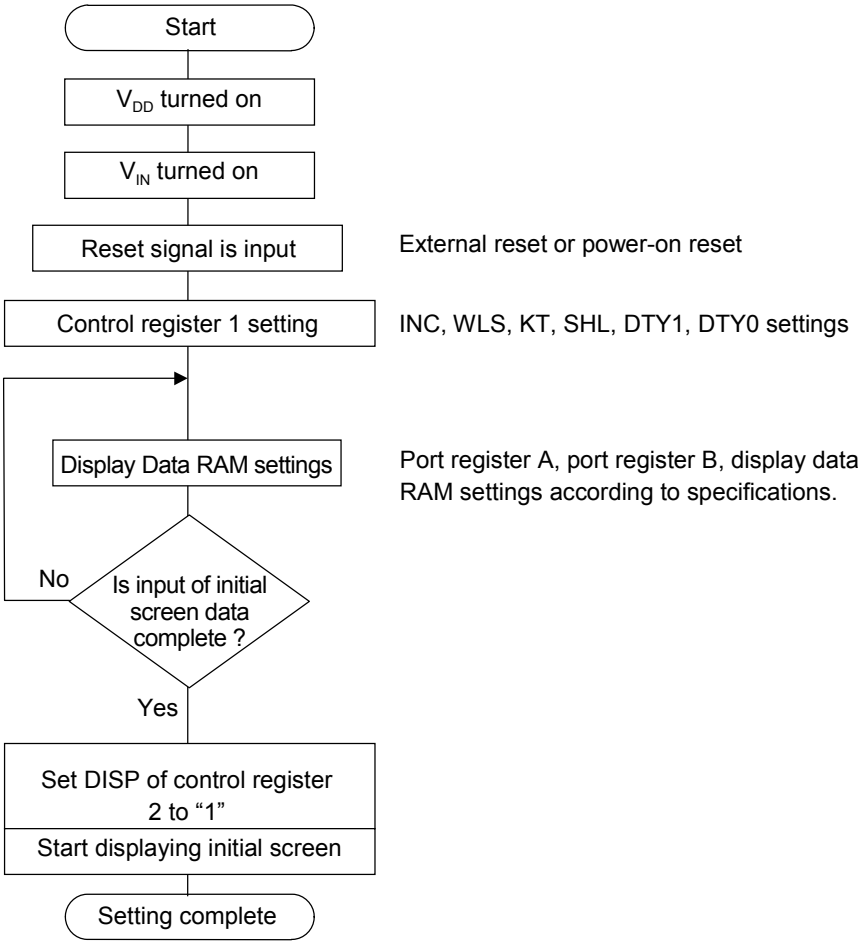


Liquid Crystal Driving Waveform Example (6)

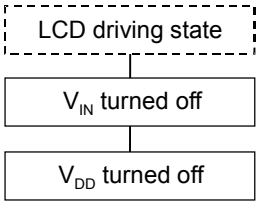
1/18 duty (1/5 bias) (ML9090A-02)



Power-On Flowchart



Power-Off Flowchart



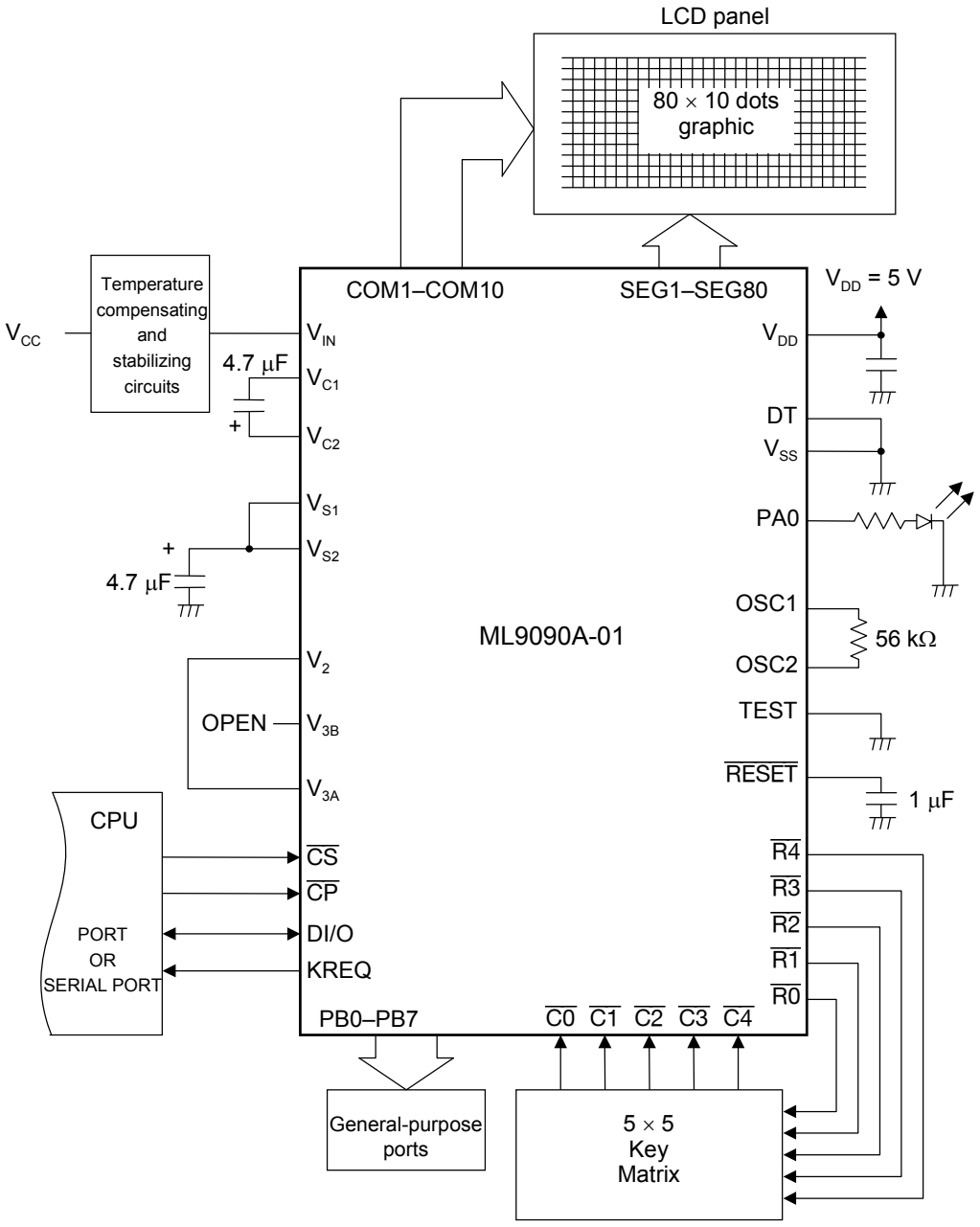
[Cautions]

- When the power supply is ON or OFF, the following power supply sequence should be used.
  At the time of power supply ON:
  Logic power supply ON → multiplied reference supply voltage (V_{IN}) ON
  At the time of power supply OFF:
  Multiplied reference supply voltage (V_{IN}) OFF → logic power supply OFF or both OFF

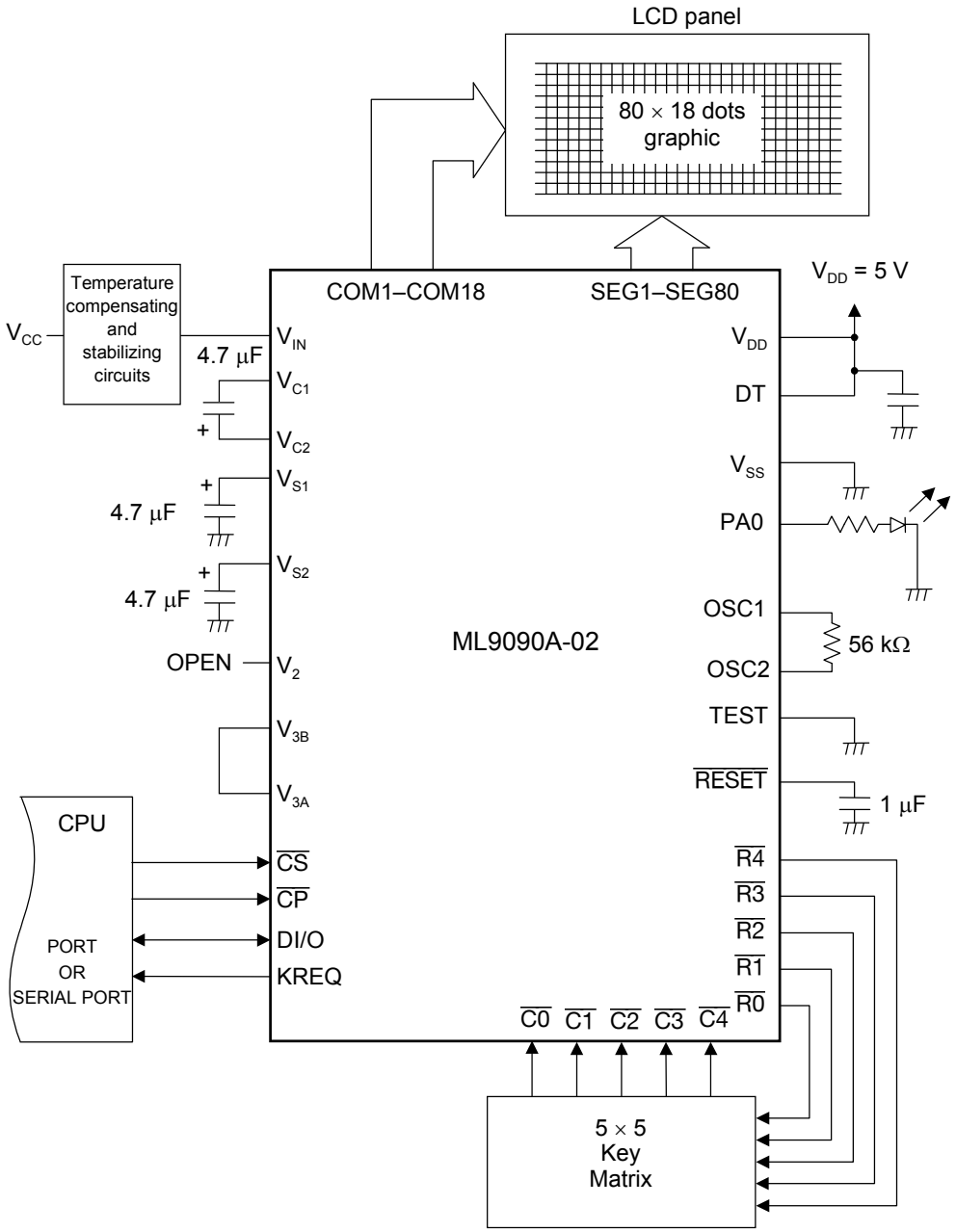
- The lines between output pins, and between output pins and other pins (input pins, I/O pins or power supply pins), should not be short circuited.

APPLICATION CIRCUIT

Application Example 1 (1/10 duty, 1/4 bias, voltage doubler)



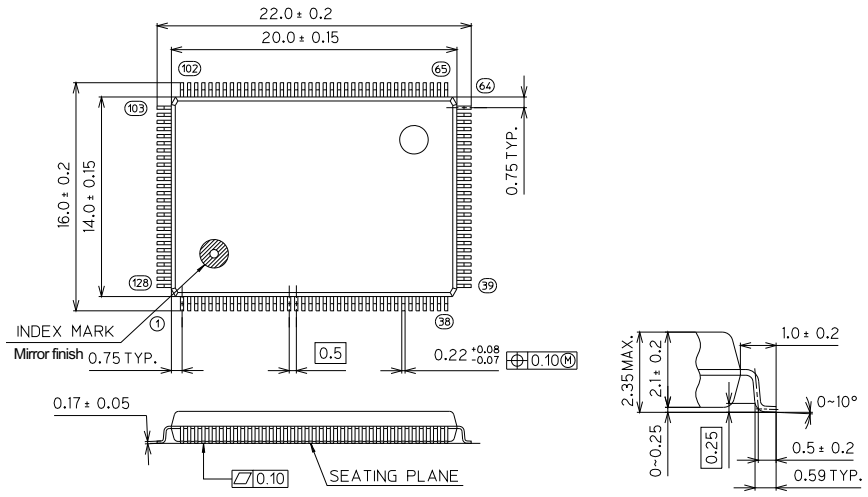
Application Example 2 (1/18 duty, 1/5 bias, voltage tripler)



PACKAGE DIMENSIONS

(Unit: mm)

QFP128-P-1420-0.50-K



LAPIS Semiconductor Co.,Ltd.

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	1.19 TYP.
Rev. No./Last Revised	4/Nov. 28, 1996

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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