dsPIC33FJ32MC202/204 and dsPIC33FJ16MC304 Family Silicon Errata and Data Sheet Clarification

The dsPIC33FJ32MC202/204 and dsPIC33FJ16MC304 family devices that you have received conform functionally to the current Device Data Sheet (DS70283**K**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33FJ32MC202/204 and dsPIC33FJ16MC304 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A6**).

Data Sheet clarifications and corrections start on page 12, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 3 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 3 programmer/debugger or PICkit 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various dsPIC33FJ32MC202/204 and dsPIC33FJ16MC304 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)				
		A2	A3	A4	A5	A6
dsPIC33FJ32MC202	0x0F09	0x3001	0x3002	0x3004	0x3005	0x3006
dsPIC33FJ32MC204	0x0F0B					
dsPIC33FJ16MC304	0x0F03					

Note 1: The Device and Revision IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory.

2: Refer to the *"dsPIC33F/PIC24H Flash Programming Specification"* (DS70152) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)				
				A2	A3	A4	A5	A6
JTAG	Flash Programming	1.	JTAG programming does not work.	X	X	X	X	X
UART	High-Speed Mode	2.	The auto-baud feature may not calculate the correct baud rate when the Baud Rate Generator (BRG) is set up for 4x mode.	X	X	X	X	X
UART	Auto-Baud	3.	With the auto-baud feature selected, the Sync Break character (0x55) may be loaded into the FIFO as data.	X	X	X	X	X
UART	Auto-Baud	4.	The auto-baud feature measures baud rate inaccurately for certain baud rate and clock speed combinations.	X	X	X	X	X
UART	Auto-Baud	5.	When an auto-baud is detected, the receive interrupt may occur twice.	X	X	X	X	X
UART	IR Mode	6.	The 16x baud clock signal on the BCLK pin is present only when the module is transmitting.	X	X	X	X	X
UART	High-Speed Mode	7.	When the UART is in 4x mode (BRGH = 1) and using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one.	X	X	X	X	X
SPI	SCKx Pins	8.	The SPIxCON1 DISSCK bit does not influence port functionality.	X	X	X	X	X
I^2C™	SFR Writes	9.	The BCL bit in I2CxSTAT can be cleared only with 16-bit operation and can be corrupted with 1-bit or 8-bit operations on I2CxSTAT.	X	X	X	X	X
I^2C	10-Bit Addressing	10.	When the I^2C module is configured for 10-bit addressing using the same address bits (A10 and A9) as other I^2C devices, A10 and A9 bits may not work as expected.	X	X	X	X	X
Product Identification	Extended Temperature	11.	Revision A2 devices marked as Extended temperature range (E) devices support only Industrial temperature range (I).	X				
UART	Interrupts	12.	The UART error interrupt may not occur, or may occur at an incorrect time, if multiple errors occur during a short period of time.	X	X	X	X	X
UART	IR Mode	13.	When the UART module is operating in 8-bit mode (PDSEL<1:0> = 0x) and using the IrDA® encoder/ decoder (IREN = 1), the module incorrectly transmits a data payload of 80h as 00h.	X	X	X	X	X
Internal Voltage Regulator	Sleep Mode	14.	When the VREGS bit (RCON<8>) is set to a logic '0', device may reset and higher Sleep current may be observed.	X	X	X	X	X
PSV Operations	—	15.	An address error trap occurs in certain addressing modes when accessing the first four bytes of any PSV page.	X	X	X	X	X
I^2C	10-Bit Addressing	16.	When the I^2C module is configured as a 10-bit slave with an address of 0x02, the I2CxRCV register content for the lower address byte is 0x01 rather than 0x02.	X	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)				
				A2	A3	A4	A5	A6
I2C	—	17.	With the I2C module enabled, the PORT bits and external interrupt input functions (if any) associated with SCLx and SDAx pins will not reflect the actual digital logic levels on the pins.	X	X	X	X	X
I2C	10-Bit Addressing	18.	The 10-bit slave does not set the RBF flag or load the I2CxRCV register, on address match if the Least Significant bits (LSbs) of the address are the same as the 7-bit reserved addresses.	X	X	X	X	X
I2C	—	19.	After the ACKSTAT bit is set when receiving a NACK, it may be cleared by the reception of a Start or Stop bit.	X	X	X	X	X
CPU	EXCH Instruction	20.	The EXCH instruction does not execute correctly.	X	X	X	X	X
PWM	Debug Mode	21.	PTMR does not keep counting down after halting code execution in Debug mode.	X	X	X	X	X
PWM	Doze Mode	22.	The Motor Control PWM module generates more interrupts than expected when Doze mode is used and the output postscaler value is different than 1:1.	X	X	X	X	X
QEI	Interrupts	23.	The QEI module does not generate an interrupt in a particular overflow condition.	X	X	X	X	X
PGEC3/PGED3 Programming Pins	Device Programming	24.	When using the PGEC3/PGED3 pins for device programming, the programming time may be slower as compared to other available PGECx/PGEDx pin pairs.	X	X	X	X	X
UART	Break Character Generation	25.	The UART module will not generate back-to-back Break characters.	X	X	X	X	X
QEI	Timer Gated Accumulation Mode	26.	When timer gated accumulation is enabled, the QEI does not generate an interrupt on every falling edge.	X	X	X	X	X
QEI	Timer Gated Accumulation Mode	27.	When timer gated accumulation is enabled and an external signal is applied, the POSCNT increments and generates an interrupt after a match with MAXCNT.	X	X	X	X	X
ADC	Current Consumption in Sleep Mode	28.	If the ADC module is in an enabled state when the device enters Sleep mode, the power-down current (IPD) of the device may exceed the device data sheet specifications.	X	X	X	X	X
All	150ºC Operation	29.	These revisions of silicon only support 140ºC operation instead of 150ºC for high-temperature operation.	X	X	X	X	
CPU	Interrupt Disable	30.	When a previous DISI instruction is active (i.e., the DISICNT register is non-zero), and the value of the DISICNT register is updated manually, the DISICNT register freezes and disables interrupts permanently.	X	X	X	X	X
CPU	div.sd	31.	When using the div.sd instruction, the Overflow bit is not getting set when an overflow occurs.	X	X	X	X	X
UART	TX Interrupt	32.	A Transmit (TX) interrupt may occur before the data transmission is complete.	X	X	X	X	X
JTAG	Flash Programming	33.	JTAG Flash programming is not supported.	X	X	X	X	X
UART	Transmit Mode	34.	TRMT bit is set before the Shift register is empty.	X	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A6**).

1. Module: JTAG

JTAG programming does not work.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

2. Module: UART

The auto-baud feature may not calculate the correct baud rate when the High Baud Rate Enable bit, BRGH, is set. With the BRGH bit set, the baud rate calculation used is the same as BRG = 0.

Work around

If the auto-baud feature is needed, use the Low Baud Rate mode by clearing the BRGH bit.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

3. Module: UART

With the auto-baud feature selected, the Sync Break character (0x55) may be loaded into the FIFO as data.

Work around

To prevent the Sync Break character from being loaded into the FIFO, load the UxBRG register with either 0x0000 or 0xFFFF prior to enabling the auto-baud feature (ABAUD = 1).

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

4. Module: UART

The auto-baud feature may miscalculate for certain baud rate and clock speed combinations, resulting in a BRG value that is greater than or less than the expected value by 1. This may result in reception or transmission failures.

Work around

Test the auto-baud rate at various clock speed and baud rate combinations that would be used in an application. If an inaccurate BRG value is generated, manually correct the baud rate in user software.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

5. Module: UART

When an auto-baud is detected, the receive interrupt may occur twice. The first interrupt occurs at the beginning of the Start bit and the second after reception of the Sync field character.

Work around

If an extra interrupt is detected, ignore the additional interrupt.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

6. Module: UART

When the UART is configured for IR interface operations (UxMODE<9:8> = 11), the 16x baud clock signal on the BCLK pin is present only when the module is transmitting. The pin is Idle at all other times.

Work around

Configure one of the output compare modules to generate the required baud clock signal when the UART is receiving data or in an Idle state.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

7. Module: UART

When the UART is in 4x mode (BRGH = 1) and using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one.

This issue does not affect the other UART configurations.

Work around

Use the 16x baud rate option (BRGH = 0) and adjust the baud rate accordingly.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

8. Module: SPI

When the SPI module is enabled, setting the DISSCK bit in the SPIxCON1 register does not allow the user application to use the SCKx pin as a general purpose I/O pin.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

9. Module: I²C

The BCL bit in I2CxSTAT can be cleared only with 16-bit operation and can be corrupted with 1-bit or 8-bit operations on I2CxSTAT.

Work around

Use 16-bit operations to clear BCL.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

10. Module: I²C

If there are two I²C devices on the bus, one of them is acting as the Master receiver and the other as the Slave transmitter. Suppose that both devices are configured for 10-Bit Addressing mode, and have the same value in the A10 and A9 bits of their addresses. When the Slave select address is sent from the Master, both the Master and Slave Acknowledges it. When the Master sends out the read operation, both the Master and the Slave enter into Read mode and both of them transmit the data. The resultant data will be the ANDing of the two transmissions.

Work around

Use different addresses including the higher two bits (A10 and A9) for different modules.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

11. Module: Product Identification

Revision A2 devices marked as Extended temperature range (E) devices support only the Industrial temperature range (I).

Work around

Use Revision A3 or newer devices marked as Extended temperature range (E) devices.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X							

12. Module: UART

The UART error interrupt may not occur, or may occur at an incorrect time, if multiple errors occur during a short period of time.

Work around

Read the error flags in the UxSTA register whenever a byte is received to verify the error status. In most cases, these bits will be correct, even if the UART error interrupt fails to occur.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

13. Module: UART

When the UART is operating in 8-bit mode (PDSEL<1:0> = 0x) and using the IrDA encoder/ decoder (IREN = 1), the module incorrectly transmits a data payload of 80h as 00h.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

14. Module: Internal Voltage Regulator

When the VREGS bit (RCON<8>) is set to a logic '0', the device may reset and a higher Sleep current may be observed.

Work around

Ensure the VREGS bit (RCON<8>) is set to a logic '1' for device Sleep mode operation.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

15. Module: PSV Operations

An address error trap occurs in certain addressing modes when accessing the first four bytes of a PSV page. This occurs only when using the following addressing modes:

- MOV.D
- Register Indirect Addressing (Word or Byte mode) with pre/post-decrement

Work around

Do not perform PSV accesses to any of the first four bytes using the above addressing modes. For applications using the C language, MPLAB C30 Version 3.11 or higher, provides the following command-line switch that implements a work around for the erratum.

```
-merrata=psv_trap
```

Refer to the readme.txt file in the MPLAB C30 v3.11 toolsuite for further details.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

16. Module: I^2C

When the I^2C module is configured as a 10-bit slave with an address of 0x02, the I2CxRCV register content for the lower address byte is 0x01, rather than 0x02; however, the module Acknowledges both address bytes.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

17. Module: I²C

With the I²C module enabled, the PORT bits and external interrupt input functions (if any) associated with the SCLx and SDAx pins do not reflect the actual digital logic levels on the pins.

Work around

If the SDAx and/or SCLx pins need to be polled, these pins should be connected to other port pins in order to be read correctly. This issue *does not* affect the operation of the I²C module.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

18. Module: I²C

In 10-Bit Addressing mode, some address matches do not set the RBF flag or load the I2Cx Receive register, I2CxRCV, if the lower address byte matches the reserved addresses. In particular, these include all addresses with the form 'xx0000xxxx' and 'xx1111xxxx', with the following exceptions:

- '001111000x'
- '011111001x'
- '101111010x'
- '111111011x'

Work around

Ensure that the lower address byte in 10-Bit Addressing mode does not match any 7-bit reserved addresses.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

19. Module: I²C

When the I²C module is operating in either Master or Slave mode, after the ACKSTAT bit is set when receiving a NACK, it may be cleared by the reception of a Start or Stop bit.

Work around

Store the value of the ACKSTAT bit immediately after receiving a NACK.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

20. Module: CPU

The EXCH instruction does not execute correctly.

Work around

If writing source code in assembly, the recommended work around is to replace:

```
EXCH Wsource, Wdestination
```

with:

```
PUSH Wdestination
MOV  Wsource, Wdestination
POP  Wsource
```

If using the MPLAB C30 C compiler, specify the compiler option: `-merrata=exch` (*Project > Build Options > Projects > MPLAB C30 > Use Alternate Settings)*.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

21. Module: PWM

If the PTDIR bit is set (when PTMR is counting down), and the CPU execution is halted (after a breakpoint is reached), PTMR will start counting up as if PTDIR was zero.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

22. Module: PWM

When the device is operated in Doze mode and the Motor Control PWM module has a postscaler set to any value different than 1:1 (PTOPS > 0 in the PxTCON register), the Motor Control PWM module generates more interrupts than expected.

Work around

Do not use Doze mode with the Motor Control PWM if the time base output postscaler is different than 1:1 (PTOPS > 0 in the PxTCON register).

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

23. Module: QEI

The Quadrature Encoder Interface (QEI) module does not generate an interrupt when MAXCNT is set to 0xFFFF and the following events occur:

1. POSCNT underflows from 0x0000 to 0xFFFF.
2. POSCNT stops.
3. POSCNT overflows from 0xFFFF to 0x0000.

This sequence of events occurs when the motor is running in one direction, which causes POSCNT to underflow to 0xFFFF. Then, if the motor stops and starts running in the opposite direction, an overflow from 0xFFFF to 0x0000 will be generated. The QEI module does not generate an interrupt when this condition occurs.

Work around

To prevent this condition from occurring, set MAXCNT to 0x7FFF, which will cause an interrupt to be generated by the QEI module.

In addition, a global variable could be used to keep track of bit 15, so that when an overflow or underflow condition is present on POSCNT, the variable will toggle bit 15. Example 1 shows the code required for this global variable.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

24. Module: PGEC3/PGED3 Programming Pins

When using the PGEC3/PGED3 pins for device programming, the programming time may be slower as compared to other available PGECx/PGEDx pin pairs, because the Enhanced In-Circuit Serial Programming™ (ICSP™) algorithm cannot be executed on this pin pair.

Refer to the *"dsPIC33F/PIC24H Flash Programming Specification"* (DS70152) for additional information on this limitation.

Work around

Use alternate PGECx/PGEDx programming pin pairs.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

EXAMPLE 1:

```
unsigned int POSCNT_b15 = 0;
unsigned int Motor_Position = 0;

int main(void)
{
            // ... User's code

            MAXCNT = 0x7FFF;       // Instead of 0xFFFF

            Motor_Position = POSCNT_b15 + POSCNT;

            // ... User's code
}
void __attribute__((__interrupt__)) _QEIInterrupt(void)
{
            IFSxbits.QEIIF = 0;    // Clear QEI interrupt flag
                                   // x=2 for dsPIC30F
                                   // x=3 for dsPIC33F
            POSCNT_b15 ^= 0x8000;  // Overflow or Underflow
}
```

25. Module: UART

The UART module will not generate consecutive Break characters. Trying to perform a back-to-back Break character transmission will cause the UART module to transmit the dummy character used to generate the first Break character instead of transmitting the second Break character. Break characters are generated correctly if they are followed by non-Break character transmission.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

26. Module: QEI

When the TQCS and TQGATE bits in the QEIxCON register are set, a QEI interrupt should be generated after an input pulse on the QEA input. This interrupt is not generated in the affected silicon.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

27. Module: QEI

When the TQCS and TQGATE bits in the QEIxCON register are set, the POSCNT counter should not increment, but erroneously does, and if allowed to increment to match MAXCNT, a QEI interrupt will be generated.

Work around

To prevent the erroneous increment of POSCNT while running the QEI in Timer Gated Accumulation mode, initialize MAXCNT = 0.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

28. Module: ADC

If the ADC module is in an enabled state when the device enters Sleep mode as a result of executing a PWRSAV #0 instruction, the device power-down current (I_{PD}) may exceed the specifications listed in the device data sheet. This may happen even if the ADC module is disabled by clearing the ADON bit prior to entering Sleep mode.

Work around 1:

In order to remain within the I_{PD} specifications listed in the device data sheet, the user software must completely disable the ADC module by setting the ADC module disable bit in the corresponding Peripheral Module Disable register (PMDx), prior to executing a PWRSAV #0 instruction.

Note: The ADC module must be re-initialized by the user application before resuming ADC operation.

Work around 2:

If the ADC module was previously initialized and enabled before entering Sleep, execute the lines of code provided in Example 2.

Note: Unlike **Work around 1**, the user application does not need to re-initialize the ADC module; however, it is necessary to re-enable the ADC module by setting the ADON bit after waking from Sleep.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

EXAMPLE 2:

```
AD1CON1bits.ADON = 0;             //Disable the ADC module
__asm__ volatile ("REPEAT #50");  //Wait 50 Tcy
__asm__ volatile ("NOP");         //Repeat NOP 51 times
Sleep();                          // Execute PWRSAV #0 and go to Sleep
```

29. Module: All

The affected silicon revisions listed below are not warranted for operation at +150ºC.

Work around

Only use the affected revisions of silicon for the high-temperature operating range, from -40ºC to +140ºC.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X				

30. Module: CPU

When a previous `DISI` instruction is active (i.e., the DISICNT register is non-zero), and the value of the DISICNT register is updated manually, the DISICNT register freezes and disables interrupts permanently.

Work around

Avoid updating the DISICNT register manually. Instead, use the `DISI #n` instruction with the required value for 'n'.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

31. Module: CPU

When using the Signed 32-by-16-bit Division instruction, `div.sd`, the Overflow bit does not always get set when an overflow occurs.

Work around

Test for and handle overflow conditions outside of the `div.sd` instruction.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

32. Module: UART

When using UTXISEL<1:0> = `01` (interrupt when last character is shifted out of the Transmit Shift Register) and the final character is being shifted out through the Transmit Shift Register, the Transmit (TX) interrupt may occur before the final bit is shifted out.

Work around

If it is critical that the interrupt processing occur only when all transmit operations are complete, hold off the interrupt routine processing by adding a loop at the beginning of the routine that polls the Transmit Shift Register Empty bit (TRMT) before processing the rest of the interrupt.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

33. Module: JTAG

JTAG Flash programming is not supported.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

34. Module: UART

When the UART is in Transmit mode, the TRMT bit may be set before the Shift register is empty. In back-to-back transmission, if the data is loaded into the U1TXREG register when the TRMT bit is set, the new byte transmission starts immediately and the Stop bit may be abbreviated, as shown in the condition below:

- When BRGH (U1MODE<3>) = 1, the Stop bit will be shortened by 1/4th of a baud rate period.
- When BRGH (U1MODE<3>) = 0, the Stop bit will be shortened by 1/16th of a baud rate period.

Work around

When using the TRMT bit to load the U1TXREG, after the TRMT bit is set, insert a delay, as defined below, before loading the U1TXREG.

When the TRMT bit is set:

- If BRGH = 1, insert a delay of at least 1/4th of the baud rate period before loading U1TXREG.
- If BRGH = 0, insert a delay of at least 1/16th of the baud rate period before loading U1TXREG.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70283**K**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Electrical Characteristics

The specifications for F21a in Table 24-19 have been updated as shown in **bold** below.

TABLE 24-19: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
	LPRC @ 32.768 kHz(1,2)						
F21a	LPRC	**-20**	**±10**	**+20**	%	-40°C ≤ TA ≤ +85°C	VDD = 3.0-3.6V
F21b	LPRC	-40	—	+40	%	-40°C ≤ TA ≤ +125°C	VDD = 3.0-3.6V

Note 1: Change of LPRC frequency as VDD changes.

2: LPRC impacts the Watchdog Timer Time-out Period (TWDT1). See Section 19.4 “Watchdog Timer (WDT)” for more information.

2. Module: 19.0 Universal Asynchronous Receiver Transmitter (UART)

In Section 19.0, a note is added above Figure 19-1:

Note:	This note applies to the applications using the UART module for LIN/J2602 applications. The LIN/J2602 standard specifies that the inter-byte space should be a non-negative number. The inter-byte space is defined as the time between the end of the Stop bit of the preceding data and the start of the following data. It is recommended to load the data to the U1TXREG after the received Stop bit is completed. Due to the half-duplex nature of the LIN/J2602 transceiver, failing to provide non-negative inter-byte space will result in a truncated Stop bit. The loading of U1TXREG after the receive interrupt should be delayed ¾ of the Stop bit time.

APPENDIX A: REVISION HISTORY

Rev A Document (4/2009)

Initial release of this document; issued for revision A2, A3, A4 and A5 silicon.

Includes silicon issues 1 (JTAG), 2-7 (UART), 8 (SPI), 9-10 (I^2C), 11 (Product Identification), 12-13 (UART) 14 (Internal Voltage Regulator), 15 (PSV Operations), 16-19 (I^2C), 20 (CPU), 21-22 (PWM) and 23 (QEI).

This document replaces the following errata document:

DS80338, *"dsPIC33FJ32MC202/204 and dsPIC33FJ16MC304 Rev. A2/A3/A4 Silicon Errata"*

Rev B Document (8/2009)

Added silicon issues 24 (PGEC3/PGED3 Programming Pins), 25 (UART), 26-27 (QEI).

Rev C Document (6/2010)

Updated silicon issue 20 (CPU).

Added silicon issue 28 (ADC) and data sheet clarification 1 (DC Characteristics: I/O Pin Input Specifications).

Rev D Document (10/2010)

Updated the work around in silicon issue 28 (ADC).

Added silicon issue 29 (All).

Rev E Document (12/2010)

Added silicon revision A6 references throughout the document.

Rev F Document (3/2011)

Removed data sheet clarification issue 1.

Rev G Document (11/2011)

Added silicon issues 30 (CPU), 31 (CPU), 32 (UART), and 33 (JTAG).

Rev H Document (12/2013)

Added data sheet clarification 1 (Electrical Characteristics).

Rev J Document (4/2016)

Added silicon issue 34 (UART).

Added data sheet clarification 2 (19.0 Universal Asynchronous Receiver Transmitter (UART)).

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